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EVALUATION OF THE WAFER-LEVEL VOLTAGE RAMP TEST FOR OXIDE INTEGRITY

Steven L. Drager

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13. ABSTRACT (Maximum 200 words)

This report has two objectives. First, it provides both an overview and a critique of the Joint Electronic Devices Engineering Council (JEDEC) 14.2 Committee on Wafer Level Reliability standard, JESD-35, "Procedure for the Wafer-Level Testing of Thin Dielectrics". This procedure was developed to provide test data which are independent of the test equipment and the facility. This standard test methodology provides the integrated circuit user with a means of comparing the oxide quality between vendors. Second, this report provides an evaluation of the oxide quality of two DoD manufacturers. The test data shows that approximately ninety percent of the sampled oxides failed due to intrinsic breakdown, which indicates a high quality oxide. However, ten percent of the tested oxides exhibited early breakdown, which causes concern that the integrated circuits might fail during their expected lifetime.

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INTRODUCTION

The purpose of this report is to describe the independent verification and validation performed on the wafer level voltage ramp test procedure developed by the dielectric working group of the Joint Electronic Devices Engineering Council (JEDEC) 14.2 Committee on Wafer Level Reliability. The motivation behind testing for oxide quality is that oxide failure is the predominant failure mechanism observed in microelectronic integrated circuits (ICs) today. This validation work has been performed at the Microelectronics Wafer Level Test Facility located in the Design and Diagnostics branch of Rome Laboratory at Rome, New York.

The goal of this verification and validation process was threefold:

1. Evaluation of the wafer level oxide integrity voltage ramp test procedure being developed by the dielectric working group within the Joint Electronic Devices Engineering Council 14.2 Committee on Wafer Level Reliability as an industry standard.

2. Evaluation of the susceptibility to oxide breakdown of a representative sample of the current product available from Department of Defense (DOD) contractors.

3. Establishment of the capability to perform wafer level reliability oxide testing within the Electronics Reliability Division of Rome Laboratory.

BACKGROUND

To begin this report, some background information will be presented so that the reader may understand the importance and value of this work. The background information provided will:

1. Describe the oxide breakdown failure mechanism and explain why it presents a problem to users of microelectronic integrated circuits.

2. Provide background information on the Joint Electronic Devices Engineering Council 14.2 Committee on Wafer Level Reliability.

3. Describe the interest of Rome Laboratory in regards to oxide breakdown.

4. Detail the capability of the Microelectronics Wafer Level Test Facility.

OXIDE BREAKDOWN

Of the big three failure mechanisms; oxide breakdown, electromigration and hot carrier degradation; oxide breakdown is the predominant reliability concern of modern microelectronic integrated circuit fabrication facilities and their customers. Previously, metal systems and their susceptibility to electromigration, had been the leading reliability hazard affecting the lifetimes of integrated circuits. The use of composite metal systems, however, has greatly alleviated the concern of metal migration. The other issue, hot carrier degradation, is one of a ghost in the machine. The physics behind the degradation is known and the industry realizes that ICs are susceptible to this mechanism. Therefore, graded junction transistors have been designed to reduce the electric fields and lessen the likeliness of degradation. Yet, few field failures from this cause have been reported. This, therefore, leaves oxide breakdown as the major reliability concern which must be dealt with in the fabrication facility.

Modern microelectronic integrated circuits are increasing in die size and process complexity every year. Each new process generation increases the complexity of integrated circuits by shrinking their geometry. Hence, this allows the number of gates for a given die size to increase. Today's Very Large Scale Integration (VLSI) ICs have hundreds of thousands, if not millions, of transistors on each die. Each transistor in that circuit has a gate oxide which is susceptible to oxide breakdown. Should a gate oxide breakdown during the useful life of the integrated circuit, chances are great that a catastrophic failure (a failure which causes the integrated circuit to cease functioning) of that IC will occur. Critical paths and the probability of using that path come into play for this analysis, but proving that a chip fails with the catastrophic failure of a single gate oxide is not the intent of this work. The point is that the oxide breakdown characteristics of each and every transistor, play a large role in determining the composite reliability of an integrated circuit. The intent of this work is to demonstrate a wafer level monitoring technique, which assures that the predominant reliability concern, that of oxide breakdown, is sufficiently monitored during fabrication. This will allow quality defect-free oxides to be produced and hence, the microelectronic integrated circuits will be able to fulfill their required service life.

Now, let's explore a few characteristics of oxide breakdown. First, *oxide breakdown failures are generally classed as being caused by an* <u>*edge*</u> *or* <u>*area*</u> *defect.* This is simply the location of the breakdown in relation to the oxide. That is, the breakdown has either occurred along the edge or in the interior of the oxide. Edge defects are generally evidence of particles which are left behind during a wafer clean. Typically, the particles remaining are left next to the topology steps formed by the resist. These particles adversely affect the silicon and oxide interface in that location. Area defects are evidence of either impurities entering the oxide during its growth or asperities existing on the silicon surface. Generally, a given process will be susceptible to either edge or area defects, but not both. This is because the dominant defect type masks the weaker defect type from recognition, leaving the weaker defect type latent within the destroyed oxide.

Second, *oxide breakdown is random in nature.* Simply put, this means that it is impossible to predict when or where an oxide breakdown failure will occur. This fact, therefore, currently prevents this mechanism from being easily handled with design for reliability software. That is, the design for reliability software could not readily predict a specific oxide, within a given circuit, which could cause the circuit to fail. The software could, however, be used to warn the designer that an edge or area intensive structure would be more suitable for this specific process. This could then be used as a guideline when designing circuits for that process to try to avoid the prevalent defect type.

Finally, *oxide breakdown is a defect driven failure mode*. This means that the oxide breakdown failure occurs due to a defect in the material. This is unlike electromigration and hot carrier degradation which are mechanism driven failures. That is to say, a mechanism driven failure is caused by a fundamental physical process. For example, hot carrier degradation results from energetic carriers being injected into the gate oxide near the drain region of the transistor. This injected charge changes the transistor characteristics by increasing the threshold voltage and lowering the transconductance of the transistor. Electromigration occurs as a result of mass transport in the current stream, not defects in the material. This can then lead to opens and shorts through the formation of hillocks and voids within the metal line.

Since oxide breakdown occurs as a result of a defect in the oxide, it is imperative to control the cleanliness of the fabrication process. The fabrication process is quite complex and therefore offers many steps for the introduction of impurities. Even though contaminants are strongly controlled in the fabrication facility, through the use of clean rooms and ultrapure ingredients, defects enter into the process at all stages. It is just not possible to create a perfectly clean environment when we are talking about contaminants on the order of less than 0.5 microns. This is very important, especially with today's ever shrinking geometries. Contaminants too small to affect current geometries, can and will cause non-functional devices in the next generation geometries. Therefore, with such a large area of the integrated circuit composed of gate oxides, and contaminants able to enter during the fabrication process, a means of monitoring the finished oxide quality is a necessity.

Now that some understanding of the design and processing aspects of oxide breakdown has been imparted, lets get into the mechanism itself. So, the next question is, why do oxides experience breakdown? Although no consensus has been reached on the absolute mechanism of oxide breakdown, it is generally accepted that this breakdown is a result of charge trapping in the oxide. When the electric field across the oxide becomes greater than the oxide is capable of handling the oxide breakdown occurs. Intrinsic breakdown of a *quality* oxide occurs at an electric field of somewhere between 10 to 14 MV/cm. The quality qualifier is important, because there exist vendors whose oxides have an intrinsic breakdown in the 8 to 12 MV/cm range. This is very important to integrated circuit reliability because a 100 Angstrom oxide experiences an electric field of 5.0 MV/cm at a 5 volt supply voltage. This means that for vendors with sub-standard intrinsic breakdown characteristics the integrated circuit is operating at an electric field which is 63 percent of the intrinsic breakdown value, as opposed to a quality oxide which operates at an electric field which is 50 percent of intrinsic breakdown.

The time to breakdown, t_{BD}, of an intrinsic oxide may be determined from the following equation:

$$t_{BD} \propto \tau_o \bullet e^{G/E_{ox}} \qquad \text{Equation 1.}$$

where: τ_o is determined from the intrinsic breakdown time under an applied voltage of V_{ap},
G, a constant, is equal to 320 MV/cm,
and E_{ox} is the applied stress field.

This equation will provide a lifetime value for the oxide, given the applied field. So, for operating conditions of 5 volts and a 150 Angstrom thick oxide, the expected lifetime is 3.6×10^{27} hours. This lifetime easily exceeds the useful life of the part. However, for the same oxide at 10 volts the lifetime is reduced to 3.1×10^{6} hours. Therefore, by doubling the operating voltage, the useful life of the device has been reduced by five. Finally, for a 100 Angstrom oxide at 5 volts the expected lifetime is 1.73×10^{13} hours. So from this equation, we see that by either reducing the oxide thickness or increasing the voltage the expected oxide lifetime is reduced.

An oxide which has a defect, however, will breakdown earlier in time and at an electric field below that of an intrinsic oxide. Generally, the breakdown is believed to occur at a defect site which exists within the oxide. As mentioned before, defect sites in oxides are thought to be asperities of the silicon surface or particles within the oxide. This is quite difficult to prove, however, as the breakdown of the oxide destroys any evidence of a possible defect. So, an oxide is only as good as its weakest point, that of the defect site.

One prevalent theory on oxide breakdown is offered by Dr. Chenming Hu. His theory is called the effective thinning model [1]. The effective thinning model explains oxide breakdown by equating the oxide thickness of a defect-free oxide and the effective oxide thickness of a defect containing oxide. That is, an oxide without a defect is truly x Angstroms thick. An oxide with a defect is x minus the defect size Angstroms thick. Since the oxide with the defect reaches an equivalent electric field at a lower voltage, that oxide will reach breakdown at a lower voltage. For example, an oxide which is 200 Angstroms thick would experience an electric field of 10 MV/cm at 20 volts. An oxide whose effective thickness is 100 Angstroms (200 Angstrom oxide with a 100 Angstrom defect) would experience an electric field of 20 MV/cm with the same 20 volts on the gate. This theory provides the following equation for the time to breakdown of an oxide:

$$t_{BD} \propto \tau_o \bullet e^{G \bullet X_{eff} / V_{ox}}$$ Equation 2.

where: τ_o is determined from the intrinsic breakdown time under an applied voltage of V_{ap},

G, a constant, is equal to 320 MV/cm,

X_{eff}, the effective oxide thickness, is equal to X_{ox} - ΔX_{ox} where:

X_{ox} is the oxide thickness,

and ΔX_{ox} is the amount of oxide thinning at the localized defect spot,

and V_{ox} is the voltage across the oxide. [V_{ox} is different than the applied voltage because of band bending and the work function difference.]

One of the pressing concerns of the semiconductor industry is the increasing electric fields which oxides experience as a result of scaling oxide thickness without reduction of the supply voltage. Not only does this raise the operating conditions closer to the intrinsic oxide breakdown levels, but it raises concern about oxide degradation. This new question which is arising in the semiconductor industry is what effect the electric field, taken as a cumulative stress, has on the breakdown characteristics of the oxide. The question is, how much has the intrinsic breakdown level of the oxide been reduced by experiencing a constant field across it? Although this work has not looked into this concern, it is not only worth mentioning, but focusing some future work on.

Table 1. Oxide Electric Field and Scaling Effects.

Oxide Thickness (Angstroms)	Electric Field (MV/cm)	
	@ 5 Volts	@ 3 Volts
250	2.0	1.2
200	2.5	1.5
150	3.3	2.0
100	5.0	3.0
80	6.3	3.8

On the issue of voltage scaling, Table 1 shows the progression of oxide thickness over the last few years and the corresponding electric field for both 5 and 3 volt technologies. From the table one may see how rapidly the electric fields are approaching the intrinsic breakdown field of oxides, especially for manufacturers whose quality is not up to par. It should also be noted that the values used in Table 1 are for combinational logic. For a memory circuit, the voltages used to write cells are higher than 5 volts. The voltages used in these circuits place the electric fields experienced by the oxide near those for intrinsic breakdown.

JEDEC 14.2

Oxide stressing at fixed electric field rates has been performed for years on devices which have undergone complete fabrication and packaging. These so called classical Time Dependent Dielectric Breakdown tests take extended periods of time (usually from 2 to 12 months) to complete. This length of time means that the tests finish well after the product has reached the field or provide a lengthy delay for the product being introduced into use. To decrease this test time, tests using ramped electric field rates, which finish in several days to a few weeks, were developed for use on the packaged parts. But these devices still have undergone all of the processing and packaging steps, so that by the time the test data becomes available, other wafer lots have also undergone the same processing and packaging steps. This means that multiple wafer lots could still be defect laden, as the testing is performed after all processing is completed. For this reason, tests of short duration performed at the wafer level during the fabrication process have been sought to monitor oxide quality. This type of test will reduce production costs by giving process engineers the ability to catch problems on a real-time basis. So, not only has the test time been significantly reduced, but the number of wafers affected by poor quality will also be greatly reduced.

Several of these wafer level oxide test implementations have been evaluated by the JEDEC 14.2 dielectric working group to be *the* industry standard fast wafer level oxide test. After many technical meetings, much discussion, and lots of work performed between the meetings, the standard JESD-35, "Procedure for the Wafer-Level Testing of Thin Dielectrics," [2] test methodology was agreed upon.

In developing the standard, the JEDEC 14.2 oxide group decided that usage of both a voltage and a current ramp wafer level oxide test procedure must be allowed. Both of these procedures have been specified as the maturity of the oxide process dictates which procedure will provide the most beneficial results. As explained below, the voltage ramp test procedure is most useful on young defect laden processes, while the current ramp test procedure provides much more valuable information on a mature oxide process.

The current ramp procedure within JESD-35 is a test whereby the current is ramped while the voltage is monitored. This test will yield detailed information about the distribution of intrinsic oxides. Therefore, this ramp test is most useful for distinguishing small differences between nearly intrinsic quality gate oxides. The time required for execution of the current ramp test is relatively short at less than one minute. Since the test is begun at a moderately high current density

(i.e. significantly greater than normal operating conditions), the test does not have far to ramp until failure.

The voltage ramp procedure within JESD-35 is a test whereby the voltage is ramped while the current is monitored. The voltage ramp test is most useful when the oxide quality is unknown, as it will yield detailed information about gross defects in the oxide population. Therefore, this ramp test is most useful for estimating the defect density of a given oxide. The test time for this method is longer than with the current ramp method (at two to three minutes), because stressing begins at nominal operating fields and the ramp continues until failure. The voltage ramp test offers a broader dynamic range for being able to deal with both high and low defect density oxides.

Both of these test procedures have been evaluated and qualified throughout the standard development process by the use of round robin testing amongst the JEDEC 14.2 oxide committee participants. The round robin tests were performed to ensure that the tests were written unambiguously and independent of the equipment used for the procedure. This independence is required so that all users of the specification will extract the same information and results when the procedures are used. Several cycles of testing had to be performed as the first round robin test results showed that the specification was ambiguous and equipment dependent. The standard was rewritten and produced an unambiguous test procedure, as demonstrated in the second round robin. The test data from this round robin clearly corroborated laboratory and equipment independence. This offers assurance to the industry that any laboratory will interpret the test procedures in the same way and that test results from the JEDEC standard test will produce consistent results between laboratories.

It is important to remember that both of these test procedures yield only a relative indication of the quality of the oxide under investigation. Therefore, these wafer level tests may be used to note variations in the oxide quality from wafer lot to wafer lot, but by themselves are not able to be directly correlated to an oxide lifetime. The oxide lifetime calculation is very complicated. This calculation takes into account the transistor on and off times, switching transients and many more characteristics which these simple wafer level tests do not account for. If an oxide lifetime prediction is required, traditional Time Dependent Dielectric Breakdown tests must be performed.

ROME LABORATORY

Rome Laboratory, as the Air Force lead for C4I technology, seeks to assure that the technology used in Air Force systems is reliable and able to fulfill mission requirements. As such, the assurance of reliable electronics is paramount to the success of the Air Force. Therefore, Rome Laboratory has been a participating member of the JEDEC 14.2 task group for dielectrics, since its inception.

There is no room for unreliable electronics in military avionic systems. Peoples lives and national security are at stake. Therefore, military integrated circuits must meet stringent Mean-Time-to-Failure (MTTF) and Mean-Time-Between-Failure (MTBF) requirements, so that the avionics systems are composed of failure-free electronics. The problem was, however, that the vast array of specifications under the Qualified Parts List (QPL) standard for qualifying microelectronic circuits, while increasing their reliability, also greatly increased the cost for these circuits. These specifications utilize testing which is performed late in the fabrication process, thus increasing the final cost of the product for reasons previously noted. Therefore, the Qualified Manufacturer's List (QML) methodology was developed. This process greatly improves the assurance of quality product by following commercial practices which are best of class.. These practices move testing and monitoring to real-time procedures, so that the process engineers may ensure quality control of the line. This methodology provides in-line testing of the parts which reduces scrap, decreases test times, improves the process flow and therefore saves money.

Rome Laboratory is well known throughout the semiconductor industry for their work in failure analysis, reliability physics and microelectronic specifications and standards. As one of the pioneering research institutes in microelectronic reliability, Rome Laboratory has performed and sponsored leading edge research in semiconductor failure mechanisms, failure analysis techniques and device characterization. The reliability science performed at Rome Laboratory is more important than ever with the ever increasing changes within the semiconductor world.

MICROELECTRONIC WAFER LEVEL TEST FACILITY

The in-house wafer level reliability program began during the late stages of the Very High Speed Integrated Circuit (VHSIC) program. That has changed as the Design and Diagnostics branch is now actively pursuing research in the area of reliable fabrication. This research not only

complements the Design-for-Reliability (DFR) program, but provides the foundation upon which design for reliability is made possible. Therefore, Rome Laboratory is looking at commercial practices which are suitable for assuring reliable product, reducing test time and cost, and which reduce the overall cost of integrated circuits for the military.

The wafer level test facility utilizes a Hewlett Packard 4062B Parametric Semiconductor Test System for its measurement capability. This system is capable of performing capacitance characterization, voltage sourcing and monitoring and current sourcing and monitoring automatically under the control of a computer. The Hewlett Packard 4062B Parametric Semiconductor Test System is composed of the following component equipment pieces:

Capacitance Measurement Subsystem (CMS)
Hewlett Packard 4280A Capacitance Meter,

Switching Matrix Subsystem (SMS)
Hewlett Packard 4085A Switching Matrix,
Hewlett Packard 4084B Switching Matrix Controller,

DC Measurement Subsystem (DMS)
Hewlett Packard 4141B DC Source/Monitor Unit,

HP4062B Parametric Semiconductor Test System Controller
Hewlett Packard series 9000 236 test system controller.

The facility is capable of performing measurements on both packaged parts and wafers. The structures under test are probed using either a:

Micromanipulator 6100 manual probe station,
or an Electroglass 2001X semi-automatic probe station.

Finally, the capability exists for measurements to be made over the temperature range of -10°C to +130°C on the Electroglass 2001X semi-automatic probe station.

The pertinent specifications for the test equipment may be found in Appendix A.

TEST STRUCTURE DESIGN

This section will begin with a review of some basic concepts for the design of oxide test structures. After these concepts have been reviewed, descriptions of each of the test structures used in this work will be presented.

DESIGN CONCEPTS

Ideally, the oxide test structures used to provide information for a particular wafer run should be designed to be representative of the process and circuits which are being fabricated in that run. This implies that each distinctive circuit type should have its own test structure set to best provide information for that device. In industry, however, it is common for each fabrication facility to have its own structure set and not necessarily distinct sets for each circuit type fabbed within that facility.

There are several design ideas and constraints which should be adhered to when designing oxide test structures. A few of these will be outlined below. Appendix B of the JEDEC specification JESD-35 [2] provides a more comprehensive set of guidelines for use in the design of an oxide test structure set.

> First, in order to accurately monitor the defect density of the oxide, the total structure area which is tested is of great concern. To be able to accurately measure the defect density, a large amount of oxide area must be tested. This may be accomplished by two means. Either a smaller number of large structures or a larger number of small structures may be tested. As one may easily recognize from basic statistics, a process with a high defect density may utilize smaller area structures to accomplish defect monitoring. This is because no matter how many defects an oxide has in it, the only one which will be recognized in the analysis is the defect which breaks the oxide down. As the process improves, however, the structure size must increase to accurately measure the lower defect density. Without an appropriately sized test structure, your process control measured defect density will not correctly predict your actual oxide defect density.

Second, by emphasizing a region in which a defect might occur, identifying the problem source will be made much more readily. For example, although a single structure providing large area as well as large perimeter may be designed, it would provide confusion when the time came to improve the process, as one would experience trouble separating out the edge from the area failures. Therefore, an oxide monitoring test structure set should include structures which are area dominated as well as structures which are perimeter dominated.

Third, Kelvin contacts should be used in all test structure designs. Kelvin contacts are recommended to ensure that proper probe contact is made. Proper contact increases the assurance of the data integrity by reducing a common source of error.

Fourth, the series resistance should be kept to a minimum. Series resistance can degrade the uniformity with which the test structure experiences stress. To reduce the series resistance, long narrow polysilicon lines should not be used in the design. Also, the use of metal contacts to the polysilicon and active areas wherever possible is strongly recommended.

Finally, the structures should go through the normal processing stages and not just those associated with gate oxidation. If the test structures only undergo the oxide formation process steps, defects introduced into the process in prior fabrication steps will not be present in the test structure. This will seriously hinder any process improvement effort as defects which could be affecting breakdown will not be monitored.

VENDOR A'S TEST STRUCTURE

The layout of Vendor A's oxide test structure is shown in Figure 1. Three probe pads and the oxide capacitor which was tested are visible in this figure. The structure shown is the p capacitor test structure for this manufacturer. The capacitor is composed of the two equally sized rectangular sections seen on both sides of the center probe pad. The connection to the capacitor gate is made through the center probe pad of this structure. The other connection necessary to form the capacitor is to the p-well. This probe point is the right most probe pad seen in Figure 1. The n capacitor for this vendor is not shown, but is similar in layout. For the n capacitor, the center

probe pad is used to contact the gate and the left most probe pad for contact to the substrate.

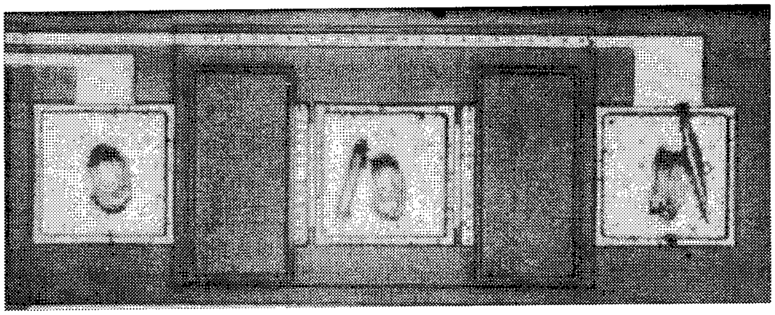

Figure 1. Vendor A capacitor test structure.

Each of the two sections which form the oxide capacitor are approximately 106 μm by 50 μm. The perimeter of this capacitor, as designed, is 624 μm. Therefore, the area of Vendor A's oxide structure is 1.0600 x 10^4 μm^2. Vendor A has used an n-well process to fabricate its devices and the nominal oxide thickness of this process was designed to be 225 Angstroms. The capacitance of this structure, as stated by the manufacturer, was designed to be 16 pF.

VENDOR B'S TEST STRUCTURE

The layout of the oxide capacitor test structure for Vendor B is shown in Figure 2. The upper center probe pad seen in this figure is the connection to the n-well. The lower center probe pad is the connection to the substrate. The upper pad left of the n-well connection is the PMOS capacitor probe point. The NMOS capacitor probe point is not shown in this picture, but is left of the leftmost upper visible pad.

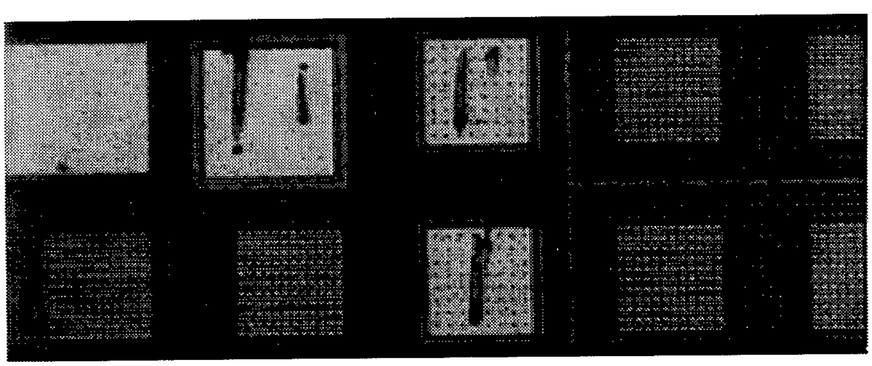

Figure 2. Vendor B capacitor test structure.

The structure for Vendor B utilizes a capacitor which is 126 μm on each side. The perimeter of this capacitor, as designed, is 504 μm. Therefore, the area of Vendor B's capacitor test structure is $1.5876 \times 10^4\ \mu m^2$. Vendor B has used a p-well process and the nominal oxide thickness was designed to be 250 Angstroms. The capacitance, as stated by the manufacturer, was designed to be 22 pF.

The structure from Vendor B varies from that of Vendor A in several respects. First, Vendor A has implemented the oxide reliability test structures in the kerf, while Vendor B utilizes a drop-in methodology for their process control measurements. The kerf is the silicon area outside of the bonding pads where the die are sawed for packaging. The drop-in methodology utilizes a die filled with test structures substituted in place of the product at that die location on the wafer. Typically, a drop-in is placed in each corner of the wafer plus a middle position, for a total of five test locations per wafer. Since the drop-in methodology allows more space for the test structures to utilize (the area of a product die versus the area in the kerf), the manufacturer may design a structure with a larger area or place a greater number of structures in the given area. Of course one may quickly see that the kerf methodology allows for fine wafer maps of the semiconductor characteristics, while the drop-in methodology will provide only a course wafer map of these characteristics.

Second, the Vendor B test structure has been designed for a large area, while the Vendor A structure has been designed for a large perimeter. Because of the limitations of working in the kerf, Vendor A chose to utilize two capacitor sections to increase his oxide test structure area and thus provide a greater perimeter. Table 2 shows a comparison of feature sizes between the test structures used by the two vendors.

Table 2. Vendor Oxide Test Structure Characteristics.

Vendor	Side x μm	Side y μm	Perimeter μm	Area $\times 10^4\ \mu m^2$	Thickness Å	Capacitance pF
A	106	50	624	1.0600	225	16
B	126	126	504	1.5876	250	22

OXIDE TEST PROCEDURE

Independent of the use of a current or voltage ramp test procedure for monitoring the oxide quality, a similar methodology is followed. Figure 3 is a flowchart of the generalized JESD-35 oxide ramp test procedure. A verbal overview of the test procedure follows. Each section of the ramp test procedure will be discussed in further detail in the sections which follow.

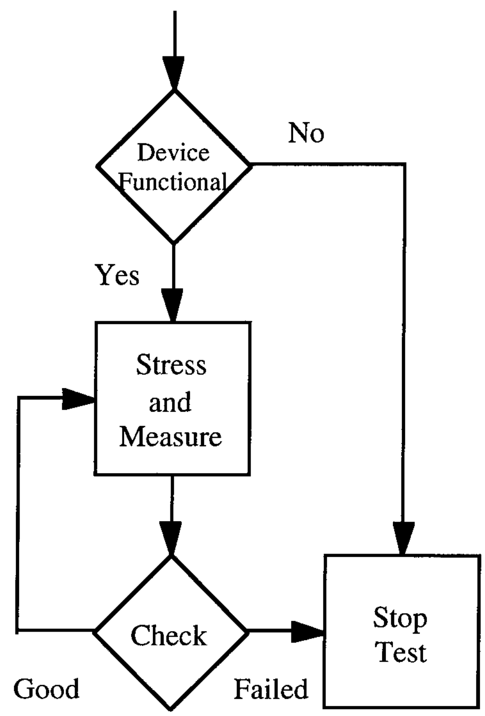

Figure 3. Generalized Ramp Test Procedure.

Step 1) The structure is checked as to its functional or non-functional status. If the device is functional, the test flow proceeds to step 2. If the device is not functional, the test is finished and the flow proceeds to step 4.

Step 2) The voltage/current stress ramp is applied to each structure which passes the functional test. The current/voltage on each structure is measured and the test flow proceeds to step 3.

Step 3) The measured value is checked and the structure is deemed either 'good,' whereby it returns to step 2 and continues the stress ramp, or 'failed,' whereby the test is finished and the flow proceeds to step 4.

Step 4) The ramp stress test is halted. The failure data point is stored. Finally, the failure is appropriately classified.

These are the general steps required to perform the wafer level oxide ramp test procedure. However, the voltage ramp stress test procedure, has an additional requirement not shown in the flowchart. Accurate knowledge of the current characteristics of the particular oxide under test must be known, as breakdown for this test procedure is defined as exceeding the expected characteristics. This knowledge may be obtained through characterization of the oxide's Fowler-Nordheim tunneling curve. This procedure will be discussed in greater detail in the Fowler-Nordheim measurement section. As breakdown of the oxide is defined by measurement in the current ramp test procedure, this predictive knowledge is not required.

The voltage ramp test procedure implemented for this work encompasses some additional features which are not called out for by the JEDEC specification. These additional steps are a direct result from the fact that our implemented test is not for a production line, but for the evaluation of product from a potential vendor. Therefore, a capacitance characterization measurement routine, step 0.5, which measures the capacitance of the unstressed oxide, has been integrated into the test procedure. The measurement of the capacitance also allows the oxide thickness of the structure under test to be calculated. Also, all voltage and current measurements during the stress ramp, as opposed to only the breakdown voltage and data classification as specified in the JEDEC test procedure, are stored.

This additional data allows parameter variances across the wafer to be monitored through the use of wafer maps. The wafer maps provide a visual method to check for variances across the wafer, trends from wafer to wafer and differences between wafer lots. Also, the additional voltage and current measurements which are stored are used to calculate the Fowler-Nordheim tunneling current curve for every oxide which undergoes testing. This is important because of the limited number of sample devices available in a non-production environment. By increasing the sample size, the accuracy with which we know the Fowler-Nordheim tunneling characteristic for the oxide under test may be increased. In a production environment where your samples are not limited, every data measurement during the test would not want to be saved, as you would quickly devour

all of your disk space.

Neither the addition of extra measurements nor storing extra data is prohibited by the JEDEC standard test procedure. No change to the intent or function of the JESD-35 standard occurs as a result of these extra steps. A complete listing of our test procedure is given in Appendix B.

FOWLER- NORDHEIM MEASUREMENT

As mentioned before, the Joint Electronic Devices Engineering Council 14.2 voltage ramp test procedure requires the knowledge of the expected current for the oxide under test. This knowledge may be obtained through application of the Fowler-Nordheim tunneling current density equation. The Fowler-Nordheim tunneling current density equation is:

$$J = Afn \bullet E_{ox}{}^{2} \bullet e^{-Bfn/E_{ox}}$$ Equation 3.

where: J is the current density in A/cm^2,

Afn is a factor in A/V^2 whose expression is given in Equation 4,

E_{ox} is the electric field in MV/cm,

and Bfn is a factor in V/cm whose expression is given in Equation 5.

The factors Afn and Bfn, in terms of the effective mass and the barrier height at the cathode, are equal to:

$$Afn = \frac{q^3 \bullet m}{16 \bullet \pi^2 \bullet \hbar \bullet m_{ox} \bullet \phi_o}$$ Equation 4.

where: q is the electron charge [1.602×10^{-19} C (Coulombs)],

m is the electron mass in free space,

m_{ox} is the electron mass in an oxide,

h is Planck's constant [6.626×10^{-34} J•s (Joule•seconds)],

ϕ_o is the barrier height in electron volts (eV).

$$Bfn = \frac{4}{3} \bullet \frac{(2 \bullet m_{ox})^{1/2}}{q \bullet \hbar} \bullet \phi_o^{3/2} \qquad \text{Equation 5.}$$

where: q is the electron charge [1.602×10^{-19} C (Coulombs)],

m_{ox} is the electron mass in an oxide,

h is Planck's constant [6.626×10^{-34} J•s (Joule•seconds)],

ϕ_o is the barrier height in electron volts (eV).

To be able to apply the Fowler-Nordheim tunneling current density equation to the oxide under test, the oxide characteristics must be known. This process begins by characterizing a sample of the oxides produced on the line. This characterization will provide *initial* values for the Afn and Bfn constants in the Fowler-Nordheim tunneling current density equation. The word initial is italicized, because it is important to continue to add characterized oxides to your database. Over time, the characteristics of the oxide may change as process improvements are implemented. As the oxides change, the Afn and Bfn factors in the Fowler-Nordheim tunneling current density equation will also change. If the voltage ramp breakdown test is not using values representing the present oxide characteristics in the determination of the failure point, then oxides which should fail at a lower voltage may not fail until a higher voltage, or oxides which should pass at low voltage may fail at these early test points. Therefore, it is important to update the oxide characteristic database with new values. Some people characterize one oxide per wafer to keep their data current. Further, some people keep the parameter calculations 'fresh' by only using recent data. For example, they only use data over the last week or month to derive the Afn and Bfn factors. Because of our limited sample sizes, we characterize an initial sample of oxides to derive the Afn and Bfn parameters. As the voltage ramp tests are performed, we translate the data into Fowler-Nordheim tunneling current data and derive the Afn and Bfn parameters as well. This then increases our characterized sample base and thus provides a better estimate.

To measure the Fowler-Nordheim tunneling current density curve for an oxide, the following procedure is performed. First, configure the oxide so that it is biased in accumulation. Second, apply a voltage ramp to the oxide with a small linear ramp rate. A rate of 0.1 MV/cm-second works well. Third, measure the current through the oxide at each voltage step. Finally, stop the ramp when the oxide has experienced breakdown.

Once the data has been collected, it is typical to plot the data with the inverse field on the x-axis and

the log of the current density divided by the electric field squared on the y-axis. The reason for plotting this combination of data will become clear with the discussion below. Figure 4 shows a typical Fowler-Nordheim tunneling current curve. The solid line, *ln(J/E²)*, plots the measured data. The large dashed line, *a_ln(J/E²)*, plots the Fowler-Nordheim tunneling current density equation. Finally, the small dashed line, *x_ln(J/E²)*, plots ten times the Fowler-Nordheim tunneling current density equation.

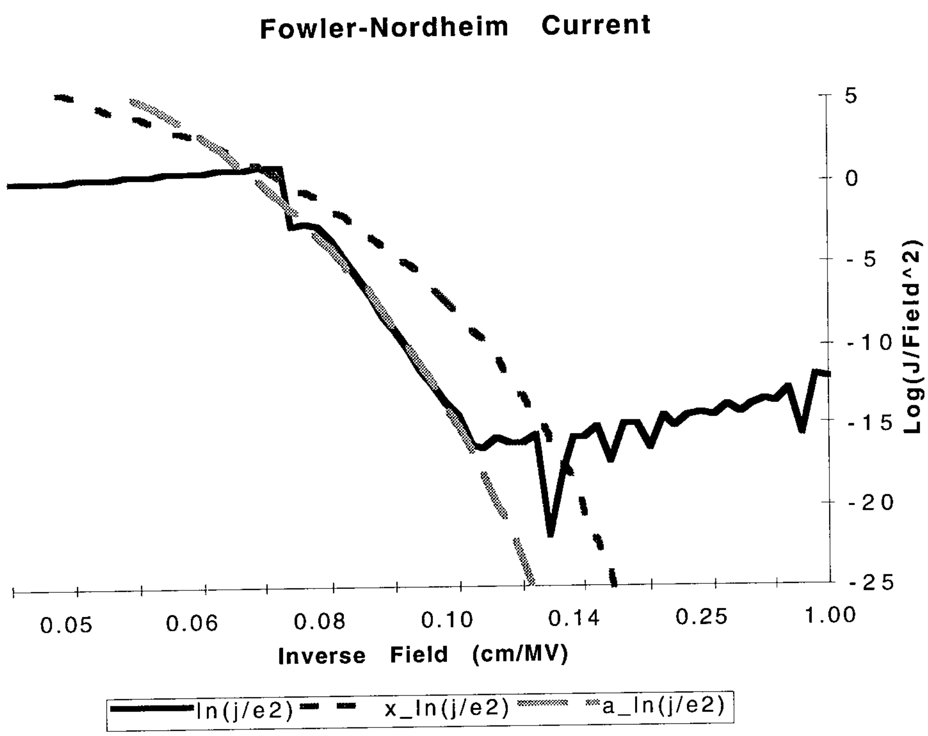

Figure 4. Fowler-Nordheim Current Plot.

To arrive at the equation of a straight line, the Fowler-Nordheim tunneling current density equation, as given in Equation 3, is transformed by:

1) Divide Equation 3 through by the electric field squared to yield:

$$J/E_{ox}{}^2 = Afn \bullet e^{-Bfn/E_{ox}} \qquad \text{Equation 6.}$$

2) Take the natural logarithm of both sides of Equation 6 to yield:

$$\ln\left(\frac{J}{E_{ox}^{2}}\right) = \ln(Afn) - \frac{Bfn}{E_{ox}}$$ Equation 7.

3) Finally, using Equation 7, the parameters defining a line (y, x, m, and b) may be seen. The parameters are listed below:

$$y = \ln\left(\frac{J}{E_{ox}^{2}}\right)$$

$$x = \frac{1}{E_{ox}}$$

$$m = -Bfn$$

$$b = \ln(Afn)$$

Therefore, once the measured data has been plotted as shown in Figure 4, Afn and Bfn become points derived from the data. By simply choosing two points from the linear portion of the Fowler-Nordheim tunneling density curve, one may determine the slope of the line and its y-intercept. From above, the slope of the line is the negative of the parameter Bfn and the y-intercept is the natural logarithm of the parameter Afn. Now all of the components of the Fowler-Nordheim tunneling current density equation are known.

Once the Afn and Bfn parameters have been obtained from the Fowler-Nordheim tunneling current density equation, the expected current for that oxide is easily obtained through application of the following equation:

$$I = A \bullet Afn \bullet E_{ox}^{2} \bullet e^{-Bfn/E_{ox}}$$ Equation 8.

where:

I is the expected current in A,
A is the capacitor area in cm,
Afn is a factor in A/V^2 whose expression is given in Equation 4,
E_{ox} is the electric field in MV/cm,
and Bfn is a factor in V/cm whose expression is given in Equation 5.

Now that the expected current for the oxide under test is known, the stopping point for the voltage ramp test may be easily determined. Simply multiply ten times the expected current to obtain the value below which the measured current must fall. This then concludes the necessary setup procedures for the voltage ramp test performed with the Fowler-Nordheim tunneling current density equation.

CAPACITANCE MEASUREMENT

This step is not defined in, nor required by, the JEDEC 14.2 procedure, but is an extra procedure which was added for several reasons. First, it verifies that proper contact with the capacitor under test is being made. Second, the measured capacitance is needed to calculate the oxide thickness. Finally, it allows plotting of wafer maps of the capacitance and oxide thickness across the wafer. These wafer maps may then be used to study the variability across the wafer, as well as make some kind of judgment about the process control of the wafers under test.

For the capacitance measurement, the capacitor should be biased in the accumulation region. This may be accomplished by placing the positive bias lead on the gate probe pad of the capacitor and the ground bias lead on the substrate/well probe pad of the capacitor. A linear stepped voltage is then used to obtain the Capacitance-Voltage (C-V) curve by stepping the voltage from a negative start value to the positive end value. In our case, the voltage range of -6.0 V to +6.0 V with a 0.5 volt step was used. The smaller the voltage step, the cleaner the C-V curve will be. However, there is a point of diminishing return where the extra test time outweighs the added information. For our testing purposes, we found the optimum step size to be 0.5 volts.

Once the capacitance measurements have been completed, a plot of this data with the voltage on the x-axis and the capacitance on the y-axis is completed. An alternative method of plotting this curve is to use the normalized capacitance, equal to C/C_{ox}, where C is the capacitance measurement and C_{ox} is the maximum capacitance measured for this particular oxide. Figures 5 and 6 show the C-V curves for a p and n capacitor respectively.

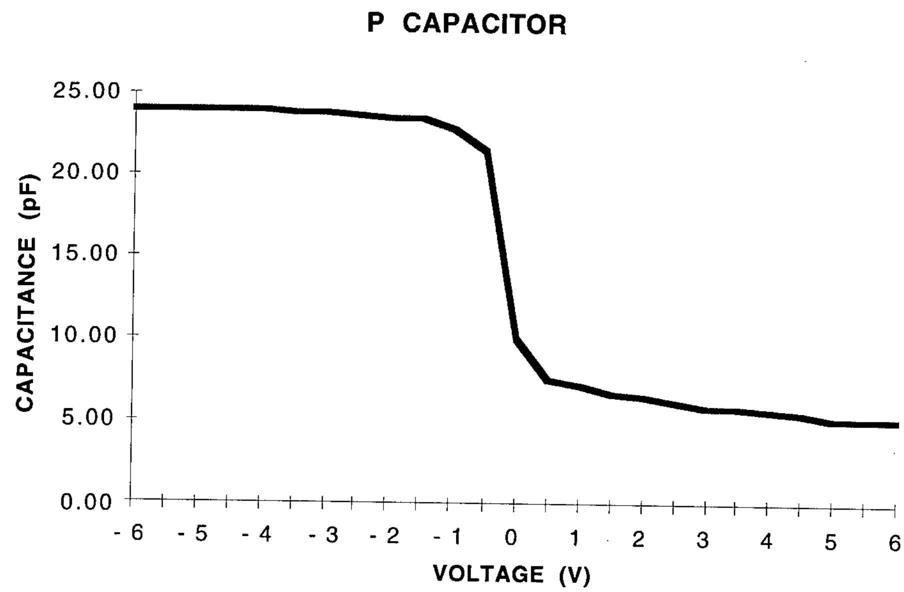

Figure 5. C-V curve for p-type MOS device.

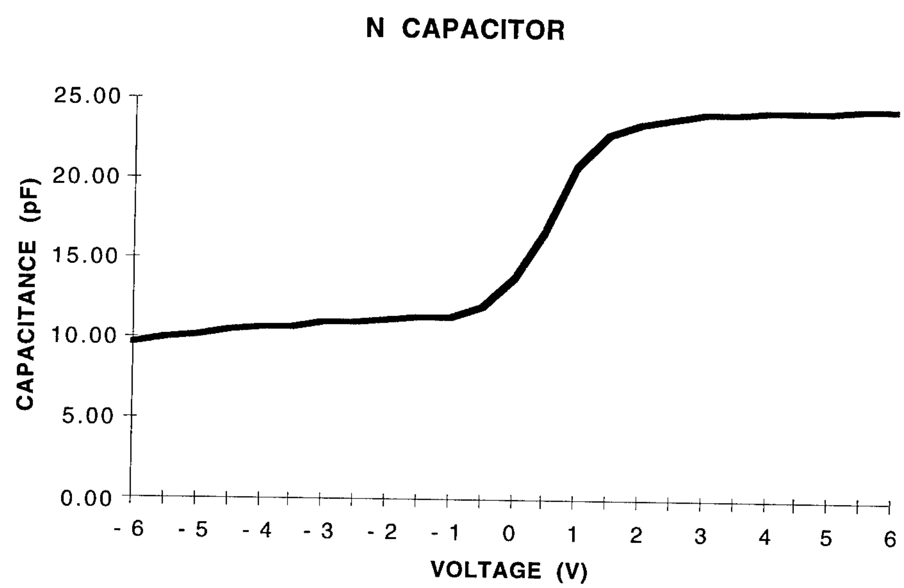

Figure 6. C-V curve for n-type MOS device.

One is able to derive the type of semiconductor with which you are working by looking at the C-V curve. A semiconductor of p-substrate, Figure 5, will display a C-V curve with accumulation at negative voltage and depletion as the voltage moves farther into the positive voltage region. A semiconductor of n-substrate, Figure 6, will display the opposite characteristic. The depletion region for a n capacitor occurs at negative voltage and goes into accumulation as the voltage

increases along the positive voltage axis.

After the measurements have been taken, the value for the capacitance may be obtained by choosing a capacitance value from the C-V curve well into the accumulation portion. The capacitance value which is chosen should be far enough into the accumulation region that the slope is almost 0. From Figure 5, the capacitance value for a voltage less than -2 volts would fulfill this requirement. From Figure 6, the capacitance value for a voltage of greater than +2 volts would fulfill this requirement.

Once the value of the capacitance is known, the oxide thickness, t_{ox} (in cm), may be calculated by using the following equation:

$$t_{ox} = \frac{\varepsilon_o \bullet \varepsilon_{ox}}{C_{ox}} \bullet A \qquad \text{Equation 9.}$$

where: ε_o is the permittivity of free space (8.85×10^{-14} F/cm),

ε_{ox} is the dielectric constant (3.9),

C_{ox} is the capacitance in Farads,

and A is the capacitor area in cm.

Now that the capacitance and oxide thickness are known, wafer maps of this data may be plotted. This is an easy visualization technique for discovering trends which may exist in the data. The trends seen on wafer maps will be due to possible problems in the processing of the gate oxide. The experimental results section will discuss any data trends seen for these parameters.

RAMP TEST PROCEDURES

The following two sections will describe the voltage and current ramp test procedures available within the JEDEC 14.2 standard wafer level oxide test procedure, JESD-35. As previously mentioned, the voltage ramp procedure should be used on a young oxide process and the current ramp used on a mature oxide process. No matter which of these test procedures is utilized, the test methodology comprises steps 1 through 3 of Figure 3. Although the current ramp procedure was not used in this work, a description of the test methodology will be provided for completeness.

This description will also allow one to compare the recommended JEDEC test procedures.

The work performed for this report utilized the voltage ramp test procedure as has been stated. This procedure was chosen for several reasons. First, the speed of the test was not a critical factor, as we are not in a production environment. Both procedures produce results within a few minutes, however, the current ramp procedure takes approximately half as long as the voltage ramp procedure. The main reason for using the voltage ramp procedure was that the oxide characteristics were unknown to us. This, therefore, required utilization of the voltage ramp procedure so gross data observability was not lost.

VOLTAGE RAMP TEST

From Step 1 of Figure 3, the first thing which must be performed upon beginning the voltage ramp test procedure is a check as to whether the structure is functional. A functional structure, for the voltage ramp test procedure, is defined as one which conducts less than 1 microampere of current at a voltage equal to the nominal operating voltage of the CMOS devices fabricated with that oxide. Therefore, non-functionality is defined as a structure which conducts greater than 1 microampere of current at the nominal operating voltage. For our case, since both vendors are utilizing 5 volt CMOS technology, the nominal operating voltage used for the functionality check was 5 volts. As with the capacitor measurement, the test capacitor must be biased in the accumulation mode. It should be noted that some people believe that this step should begin at 0 volts and not the nominal operating voltage. The reasoning is that the resolution on any early failures is lost.

The voltage ramp procedure then moves onto Step 2, which as shown in Figure 3 is the application of the voltage stress ramp and measurement of the resultant current. For this step, the voltage is ramped linearly or stepped as close to linearity as possible. The current through the oxide should either be measured continuously or at short evenly spaced intervals throughout the ramp process. If short evenly spaced intervals are used to measure the current, at least one measurement per voltage level is required. A detailed listing of the voltage ramp characteristics is presented in Table 3. Please note that additional requirements are placed on the voltage ramp characteristics if a stepped approximation to linearity is used.

Table 3. Voltage Ramp Specification Characteristics.

Ramp Rate:	0.1 to 1.0 MV/cm-s
Ramp Type:	Linear or Stepped Approximated
Maximum Time Between Current Measurements:	0.1 seconds
Maximum Electric Field Allowed:	15.0 MV/cm
Minimum Current Density Compliance Limit:	20 A/cm^2

If the stepped approximation is utilized, then the following additional constraints apply:

Maximum Voltage Step Height:	0.1 MV/cm
Step Duration:	Uniform & Consistent with Ramp Rate
Current Measurement Interval:	At least Once per Step

The final procedure in the voltage ramp section of the test is shown as Step 3 of Figure 3. This step checks the measurement data to determine if the structure continues the stress process or is removed from the stress loop. The voltage ramp test is stopped for one of two possible reasons. First, if the current increase through the capacitor is greater than ten times the expected Fowler-Nordheim current level the capacitor is removed from the stress ramp. Second, if the maximum electric field, 15 MV/cm, has been reached, the capacitor is removed from the stress ramp. When the test has reached either of these two conditions, the stress ramp is halted. The initial test is then repeated to check whether the capacitor has broken down. Once this is completed, the voltage ramp test procedure moves to Step 4, which is described in the failure classification section.

Although not called out for in the JESD-35, we have incorporated graphing of the voltage ramp data into our test program. This provides real-time feedback on the current oxide under test. Figure 7 through Figure 9 show examples of the plotting performed for a given set of voltage ramp breakdown data.

Figure 7 is the real-time plot produced as the voltage is forced onto the capacitor and the current is measured. The x-axis plots the voltage forced onto the capacitor, while the y-axis plots the log of the current which was measured. The solid line, *current*, in this plot is the actual current values which were measured from the capacitor. The large dash line, *ixptd*, represents the expected value of the current based on predictions from the Fowler-Nordheim tunneling current density equation. The small dash line, *10_ixptd*, is the voltage ramp test failure line. That is, this line represents ten times the expected current, which is one of the possible failure conditions for the voltage ramp test. It should be noted that the Fowler-Nordheim tunneling current density equation does not provide a

completely accurate prediction of the expected current. This is why Figures 8 and 9 show up.

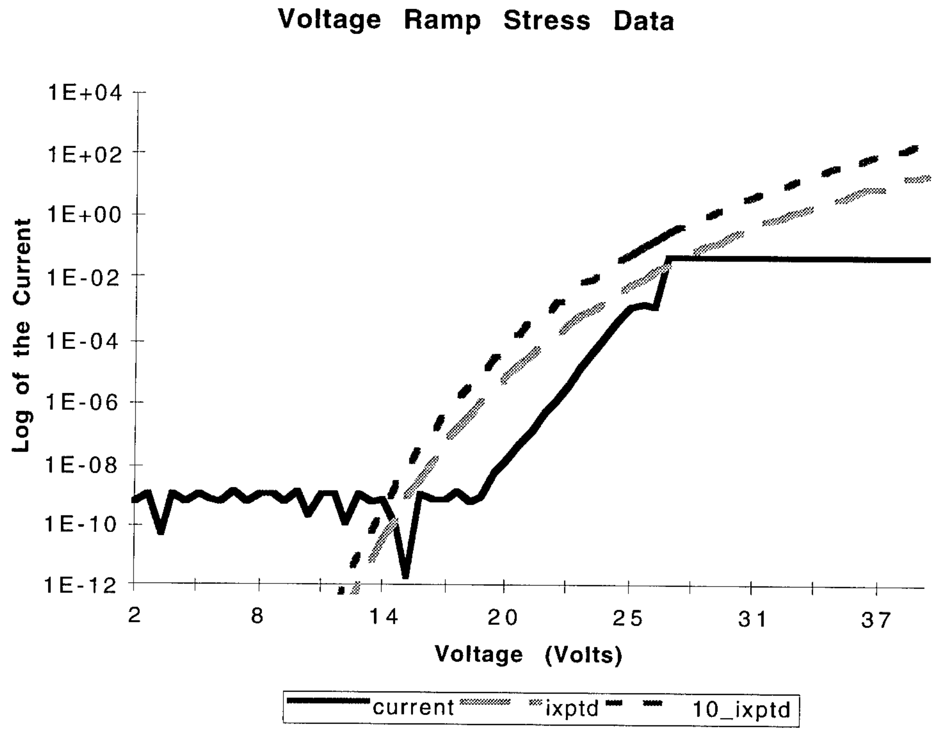

Figure 7. Voltage Ramp Stress Data and the Expected Current.

Figure 8 is a plot of the same data shown in Figure 7 except that it is now shown in the form of a Fowler-Nordheim tunneling current density plot. The solid line, *ln(J/E²)*, represents the actual data which was measured. The large dash line, *x_ln(J/E²)*, is the Fowler-Nordheim curve for that oxide. The small dash line, *a_ln(J/E2)*, is ten times the Fowler-Nordheim equation. The data has been replotted in this form so that the parameters Afn and Bfn may be derived for the oxide under test. By performing this step, the number of points from which Afn and Bfn are averaged is increased, thus increasing the statistical significance of their calculated values.

Figure 9 then replots the measured data shown in Figure 7 using the value of Afn and Bfn calculated from the Fowler-Nordheim tunneling current density curve of Figure 8. Notice how in Figure 9 the expected current, *a_ixptd*, maps onto the linear portion of the breakdown curve, *current*. Also of note is that the ten times expected curve, *a_10_ixptd*, crosses the measured data right at the point of oxide breakdown.

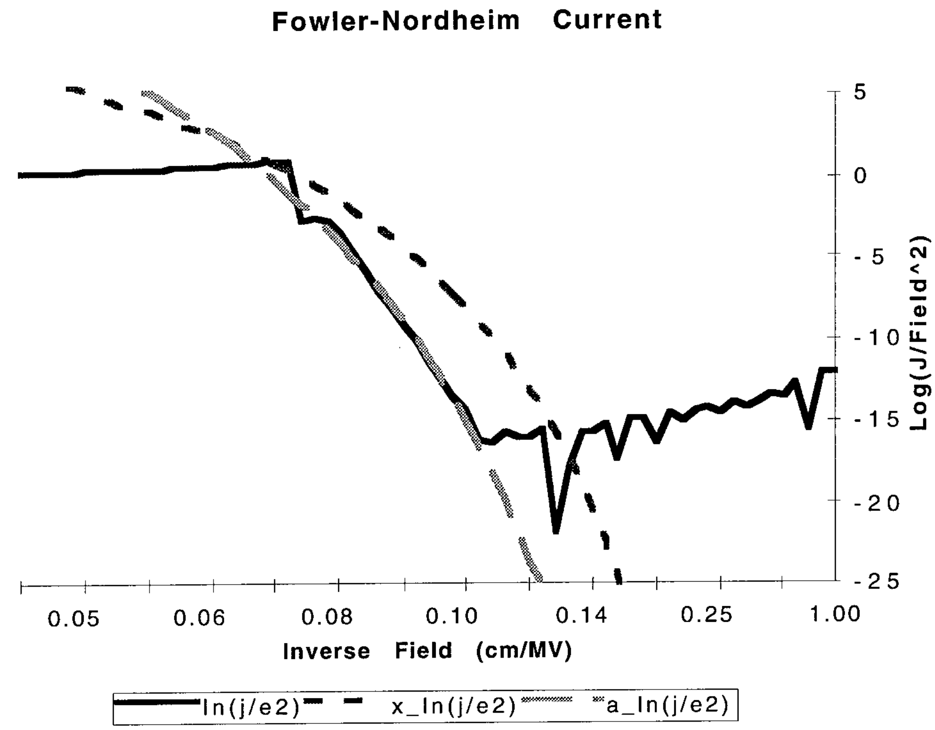

Figure 8. Fowler-Nordheim Plot of the Voltage Ramp Data.

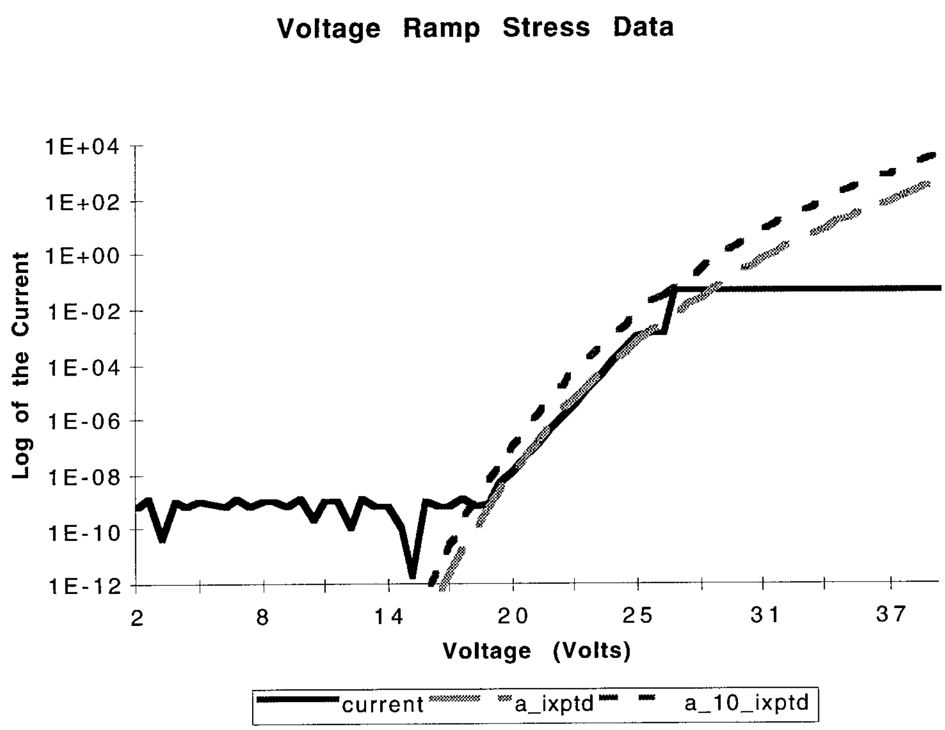

Figure 9. Voltage Ramp Stress Data and the Recalculated Expected Current.

The final aspect we have added to this section is the calculation of the breakdown field. The field across the oxide, E_{ox}, may be calculated by the following equation:

$$E_{ox} = \frac{V_{ox}}{t_{ox}} \qquad \text{Equation 10.}$$

where: V_{ox} is the voltage drop across the oxide, and t_{ox} is the oxide thickness in cm.

CURRENT RAMP TEST PROCEDURE

The current ramp test procedure is the other possible form of wafer level stressing which the JEDEC standard makes available to the user. Following the steps of Figure 3, Step 1 begins with a check to see that the structure under test is functional. This initial check is performed by applying a current, typically 1 uA, to the capacitor under test. If the capacitor does not reach use condition voltage within 50 ms, then the oxide has failed.

The current ramp procedure then moves onto Step 2, which as shown in Figure 3 is the application of the current stress ramp and measurement of the resultant voltage. For this step, a stepped current consistent with the specifications listed in Table 4 is applied, while the voltage is monitored continuously or at short evenly spaced intervals. The current should be stepped in logarithmic intervals so that the ratio of two successive steps is a constant factor, F. The maximum value which F may take on is the square root of 10, or approximately 3.2. The characteristics of the current stress ramp are:

Table 4. Current Ramp Specification Characteristics.

Current Ramp Rate:	1 decade/500 ms
Maximum Time Between Voltage Measurements:	Lesser of 50 ms or Once per Current Step
Maximum Charge Density Allowed:	50 C/cm^2
Minimum Voltage Field Compliance Limit:	15 MV/cm
Maximum Current Increase Factor (F):	Square Root of 10 (approximately 3.2)
Step Duration:	Uniform

The final procedure in the current ramp section of the test is shown as Step 3 of Figure 3. This step checks the measured data to determine if the structure continues the stress process or is removed from the stress loop. The current ramp test is stopped when the measured voltage is 0.85 times the previously measured voltage. If the voltage is being continuously monitored, the test is stopped when the present voltage is 0.85 times the highest previously measured voltage. Two other reasons also force the completion of the test. If the voltage compliance of the equipment has been reached, or if the capacitor under test has attained the maximum charge density, 50 C/cm^2, the current ramp test should also be stopped. The initial test is then repeated to check whether the capacitor has truly broken down. Once this is completed, the voltage ramp test procedure moves to Step 4, which is described in the failure classification section.

Since the current ramp test procedure has not been used on the data contained in this report, no further additions or comments will be made on this procedure.

FAILURE CLASSIFICATION

The final step of the oxide test procedure is Step 4 of Figure 3. This step is the storage and appropriate classification of the failure data. Both the voltage ramp and the current ramp require that the same information is stored. Upon completion of the ramp test portion of the procedure, the breakdown voltage (Vbd), the breakdown charge density (Qbd) and the failure classification are stored. The breakdown voltage is the maximum voltage forced on the oxide prior to breakdown or the maximum measured voltage prior to breakdown, depending on which procedure is utilized. The breakdown charge density may be calculated as the sum of the current-time products for all of the measurement intervals prior to breakdown and not including the measurement interval in which the breakdown occurred.

Table 5. JEDEC Oxide Failure Categories

Failure Category	Initial Test	Ramp Test	Post Stress
Initial	Fail	N/A	N/A
Catastrophic	Pass	Fail	Fail
Masked Catastrophic	Pass	Pass	Fail
Non-Catastrophic	Pass	Fail	Pass
Others	Pass	Pass	Pass

Table 5 provides a view of how the test structures are mapped into the failure classification

categories according to which portions of the test procedure they have failed and or passed. Each of the failure categories are described following this table. Finally, to close out this section, Figure 10 offers a view from the test procedure flow as to how the failure classifications are derived.

The first two failure categories are predictors for the yield and reliability of the devices from the fabrication facility. These categories are:

> The structures which fail the initial use condition test are grouped into the initial failure category. This category provides useful information about the defect tail. If a high percentage of the devices tested are grouped into this category, it is reasonable to assume that the functional devices will not yield. This presents a yield problem and not a reliability concern.
>
> The next category, catastrophic, is the bin of those devices which fail during the ramp test and fail the post stress check. These oxides form the population which is of interest, as these are the devices which will make it into the field. Low field breakdowns in this population are cause for a reliability concern.

The final three categories should be censored from any data analysis. However, the data from these categories should not be ignored. If only a few of the test samples fall into these categories, no real problem exists and it is alright to ignore the data. If many of the oxides are getting categorized into these groupings then it is cause for alarm. When many failures begin to be grouped into these categories, it is a sign that something has gone wrong with the test procedure and needs immediate attention. These categories are as follows:

> The masked catastrophic category are those that do not fail the ramp test, but fail the post stress check. This category is indicative of an instrument timing problem. The timing problem has caused the equipment to miss the failure during the ramp test.
>
> The non-catastrophic category is composed of those structures which fail during the ramp test but pass the post stress check. This group is indicative of an initial short occurring which has opened during the test.
>
> Finally, the others category are those that fail neither the ramp test nor the post stress check. This is indicative of a miss probing.

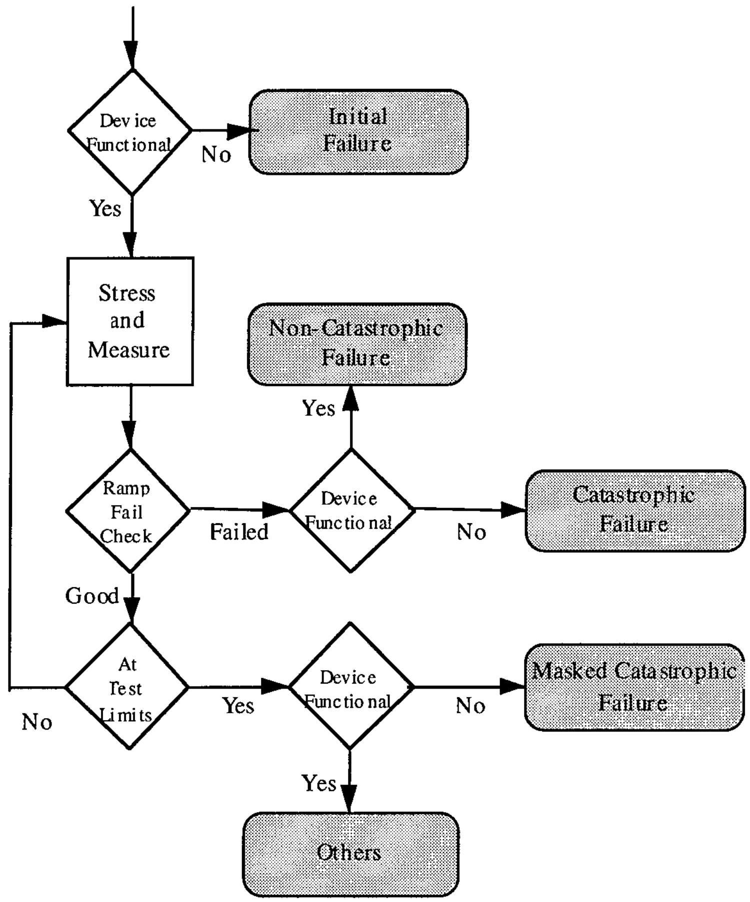

Figure 10. Failure Categories

EXPERIMENTAL RESULTS

This section will provide an overview of the experimental results recorded during this work. The data will be presented in the order discussed during the test procedure. Therefore, we will begin with the data collected during the Fowler-Nordheim procedure, continue with the data collected during the capacitance measurement and finish with the data collected during the voltage ramp procedure. Complete listings of both the measured and calculated data may be found in Appendices C through F. A summary of the contents of each appendix is listed below.

> Appendix C provides a complete listing of the raw data for each capacitor tested. The data presented includes the measured data of capacitance, pre-stress current, breakdown voltage and the calculated data for oxide thickness, breakdown field, and the Fowler-Nordheim fit parameters Afn and Bfn. Appendix B also contains the ramp rate used for each sample and the failure classification given to it.
>
> Appendix D provides a complete statistical analysis for each of the just mentioned data categories. The statistics covered include the minimum, maximum, range, summation, observation count, mean, median, mode, standard deviation, variance and a few other statistics about the data.
>
> Appendix E provides histograms for each of the measured and calculated categories for both the uncensored and the censored distributions. For Vendor A, histograms have been produced for groupings which include all of the capacitors tested, all n capacitors tested and all p capacitors tested. For Vendor B, histograms have been produced for groupings which include all capacitors tested, all wafer 1 capacitors, all wafer 2 capacitors, all n capacitors, all wafer 1 n capacitors, all wafer 2 n capacitors, all p capacitors, all wafer 1 p capacitors and all wafer 2 p capacitors.
>
> Finally, Appendix F contains the breakdown data tabulated by number of breakdowns per field for combinations of the capacitor type and ramp rate. This appendix also contains the data tabulated in cumulative breakdown format. The cumulative breakdown curves for this data are also plotted in this section.

There are a few things which should be noted about the data. Vendor A had 91 capacitors which were tested. Of these, there were 2 initial fails and 1 masked catastrophic failure. Vendor B had

207 capacitors which were subjected to the voltage ramp. Of these, there were 3 masked catastrophic failures. In the next few paragraphs, more detail about the censored data points will be presented.

Vendor A had 3 n-type devices which were censored for the censored data analysis. Two of these failures were classified as initial failures, one occurring during the initial current measurement and the other occurring within the first few ramp steps. The other failure was a masked catastrophic failure detected only once the voltage ramp was finished. Both of the censored capacitors which saw stressing and failed were being run at a rate of 1.0 MV/cm-s. There was also an additional data point censored for anomalous Fowler-Nordheim tunneling current density data.

Vendor B had 3 n-type capacitors on wafer number 1 censored. All of these device failures were of the masked catastrophic variety. Two of these censored data points were being run at a ramp rate of 0.1 MV/cm-s, while the third had a ramp rate of 0.5 MV/cm-s. An additional data point was censored from the Fowler-Nordheim tunneling current density data, as the values were deemed anomalous. It is interesting to note that none of the failures seen with Vendor B occurred to a p type capacitor or any of the n type capacitors on wafer 2.

Finally, as we only had packaged parts for Vendor A, wafer maps could only be produced from the Vendor B data. All of the wafer maps which follow in this report have been shaded in the following manner. First, the minimum and maximum values in the wafer maps were found. Second, the minimum value was subtracted from the maximum value to obtain the difference. Third, for lack of a better number, the difference was divided by four to obtain four evenly spaced intervals. Therefore, there are four bins into which the data must fall, but in no way is the data evenly distributed between the bins or was the data attempted to be evenly distributed. This method is meant to provide the ability to quickly observe any trends which may appear across the wafer. By using a greater number of bins, a more detailed analysis may be performed which may achieve a finer resolution for any trends which may exist across the wafer. Those values equal to N/A are those structures which sacrificed their lives to the development of the test procedure. Those numbers in bold are structures who wound up on the censored list of values.

FOWLER-NORDHEIM DATA

Tables 6 and 7 show the statistical breakdowns of the calculations for the Fowler-Nordheim

current density equation fit parameters, Afn and Bfn, for the two vendors used in this study.

Table 6. Vendor A Fowler-Nordheim Fit Parameter Statistics.

Statistics	Uncensored Afn	Censored Afn	Uncensored Bfn	Censored Bfn
Mean	4.09E+52	7.04E+19	500.89	490.38
Standard Error	4.09E+52	4.59E+19	16.45	9.86
Median	4.29E+14	4.82E+14	481.99	479.08
Mode	#N/A	#N/A	#N/A	#N/A
Standard Deviation	3.95E+53	4.35E+20	158.68	93.56
Variance	1.56E+107	1.89E+41	25180.67	8754.20
Kurtosis	9.30E+01	7.49E+01	32.10	-0.15
Skewness	9.64E+00	8.42E+00	4.35	0.35
Range	3.81E+54	3.97E+21	1538.45	446.83
Minimum	1.96E+05	1.96E+05	134.47	261.00
Maximum	3.81E+54	3.97E+21	1672.92	707.83
Sum	3.81E+54	6.34E+21	46583.11	44134.64
Count	9.30E+01	9.00E+01	93.00	90.00

Table 7. Vendor B Fowler-Nordheim Fit Parameter Statistics.

Statistics	Uncensored Afn	Censored Afn	Uncensored Bfn	Censored Bfn
Mean	7.22E+58	1.54E+10	327.29	316.78
Standard Error	7.22E+58	1.11E+10	7.65	4.05
Median	4.79E+07	4.73E+07	325.89	323.65
Mode	1.92E+07	1.92E+07	329.73	329.73
Standard Deviation	1.04E+60	1.58E+11	110.03	57.63
Variance	1.08E+120	2.51E+22	12107.34	3321.76
Kurtosis	2.07E+02	1.97E+02	78.66	8.58
Skewness	1.44E+01	1.39E+01	7.06	-0.92
Range	1.49E+61	2.24E+12	1476.20	529.27
Minimum	3.65E+02	3.65E+02	88.48	88.48
Maximum	1.49E+61	2.24E+12	1564.67	617.74
Sum	1.49E+61	3.12E+12	67748.66	64306.56
Count	2.07E+02	2.03E+02	207.00	203.00

Note the significant difference in the censored Afn values between the vendors. While the values for Afn vary greatly in the literature, the exponents typically range between 6 and 12. The Afn value for Vendor A is significantly outside of this region. Values for Bfn found in literature range from 210 up to 280. We have found the Bfn value for Vendor B to be 316. This value is in the ballpark of the literature values, however, Vendor A is almost double the high end of literature values. We have been unable to arrive at a plausible explanation as to why the fit parameters for Vendor A are so much out of range from the literature values.

CAPACITOR CHARACTERISTIC DATA

This section will discuss the results of the data collected during the capacitance characterization. Specifically, this section will discuss the measured capacitance values and the calculated oxide thickness.

CAPACITANCE

Table 8 is a breakdown of the mean capacitance values for the Vendor A tested oxides. The table contains both the censored and the uncensored numbers broken down by ramp rate and the type of capacitor. One may easily determine that the mean capacitance value for Vendor A is 19.13 pF. The measured mean is about three picoFarads higher than the designed to capacitance of 16 pF previously mentioned. For most of the ramp rates, the mean capacitance values of the N capacitors are lower than the mean, therefore the P capacitor values are higher than the mean.

Table 8. Vendor A Mean Capacitance Values (pF).

Rate	N		P		Total	
	uncensored	censored	uncensored	censored	uncensored	censored
0.1	19.14	19.14	19.17	19.17	19.15	19.15
0.3	19.10	19.10	19.11	19.11	19.10	19.10
0.5	19.18	19.18	18.95	18.95	19.09	19.09
0.7	18.96	18.96	19.02	19.02	18.99	18.99
1.0	19.19	19.21	19.99	19.19	19.65	19.20
all	19.13	19.14	19.30	19.12	19.22	19.13

The histograms for the Vendor A measured capacitance may be found in Appendix E, Figure 35 through Figure 42. Histograms for the uncensored and censored distributions exist for groupings of all capacitors, the n capacitors and the p capacitors. With the exception of the all and p capacitor uncensored distributions, the histograms appear to be normally distributed. The uncensored total sample p capacitor distributions do not appear to be normally distributed because of a high value which lumps the majority of the values into only two bins.

Table 9 is a breakdown of the mean capacitance values for the Vendor B oxides tested. The table contains both the uncensored and censored measured values. The values are further broken down by the ramp rate, type of capacitor and the wafer on which the tested oxide resides. One may easily see that the mean capacitance for Vendor B is 24.36 pF. The mean of the measured

capacitance is just over two picoFarads higher than the designed capacitance of 22 pF previously mentioned. For all ramp rates, the mean capacitance values of the N capacitors are higher than the mean and therefore the P capacitor values are lower than the mean. If we compare wafer 1 against wafer 2, we see that wafer 2 has the higher mean for 2 of the ramp rates. The capacitance measurements for this vendor fall into a very tight range with only a difference of 1.84 picoFarads occurring in the uncensored distribution.

Table 9. Vendor B Mean Capacitance Values (pF).

uncensored									
Rate	N1	N2	N	P1	P2	P	W1	W2	Total
0.1	24.33	24.65	24.40	24.07	24.15	24.09	24.19	24.40	24.23
0.5	24.62	24.54	24.56	24.13	23.99	24.04	24.35	24.25	24.28
1.0	24.67	24.74	24.71	24.17	24.15	24.16	24.43	24.46	24.44
all	24.56	24.65	24.61	24.13	24.08	24.10	24.34	24.36	24.35

censored									
Rate	N1	N2	N	P1	P2	P	W1	W2	Total
0.1	24.43	24.65	24.48	24.07	24.15	24.09	24.22	24.40	24.26
0.5	24.68	24.54	24.58	24.13	23.99	24.04	24.37	24.25	24.28
1.0	24.67	24.74	24.71	24.17	24.15	24.16	24.43	24.46	24.44
all	24.61	24.65	24.63	24.13	24.08	24.10	24.35	24.36	24.36

The histograms for the Vendor B measured capacitance may be found in Appendix E, Figure 65 through Figure 82. Histograms for the Vendor B data have been generated for the total capacitor population, the wafer 1 population, the wafer 2 population, the n capacitor population, the wafer 1 n population, the wafer 2 n capacitor population, the p capacitor population, the wafer 1 p capacitor population, and the wafer 2 p capacitor population. For the most part, the histograms for all of the distributions appear to be normally distributed. However, the histograms of the n capacitors should be noted. The total n capacitor curve has an elongated tail on the left side before moving into the normal distribution. This attribute seems to be picked up from the wafer 1 n capacitors, which is the population where all of the censored devices for this vendor came from.

The following four figures, Figure 11a, 11b, 12a, and 12b, are wafer maps of the measured capacitance values for the Vendor B wafers tested. These wafer maps provide an easy visual method for discovering possible quality problems. As the Vendor A tested samples were packaged, we were therefore unable to create wafer maps for their data.

Figure 11a shows the measured n-type capacitance values from the Vendor B first wafer. The three numbers in bold are the capacitors which have been censored for reasons explained in the

failure classification section. The locations marked with N/A denote the oxide capacitors who gave their life for the development of the voltage ramp stress test program. Although the regions are not clear and distinct, the data seems to be regionally distributed across the wafer. Generally, the capacitance values are higher on the top of the wafer than the bottom of the wafer. Also, the capacitance values are higher on the left side of the wafer than the right side. The differences on this wafer are not an indication of any sort of problem, but are due to the normal processing variation. The processing variations may occur due to the orientation of the wafer within the diffusion furnace. Wafers which are nearer to the source receive higher dopant concentrations and greater air flow than those at the other end of the furnace. It is probable that this wafer was not near the source end of the diffusion furnace.

			N/A	N/A			
	N/A	N/A	**23.41**	24.47	24.44	24.67	
	N/A	N/A	24.74	24.68	24.85	24.50	24.34
24.56	24.88	25.10	25.02	24.91	24.84	N/A	24.62
25.25	24.87	25.14	24.75	24.63	24.55	24.71	24.59
23.72	24.83	25.07	24.91	24.64	24.54	24.48	24.36
	24.74	25.02	24.66	24.63	24.48	24.39	24.28
	23.99	24.16	24.27	24.15	**24.05**	23.93	
			24.08	24.66			

Ranges

23.41-23.87	23.87-24.33	24.33-24.79	24.79-25.25

Figure 11a. Vendor B Wafer 1 N Capacitor Capacitance Wafer Map (pF).

			24.82	24.63			
	25.07	24.83	24.71	24.79	24.69	24.60	
	25.11	24.87	24.82	24.83	24.47	24.40	24.19
25.22	24.98	24.83	24.72	24.71	24.61	24.35	24.19
25.17	25.03	24.83	24.74	24.84	24.45	24.32	24.15
25.17	25.01	24.76	24.66	24.85	24.60	24.31	24.07
	24.81	24.80	24.80	24.58	24.37	24.27	24.06
	24.34	24.64	24.65	24.50	24.37	24.53	
			24.53	24.36			

Ranges

24.06-24.35	24.35-24.64	24.64-24.93	24.93-25.22

Figure 11b. Vendor B Wafer 2 N Capacitor Capacitance Wafer Map (pF).

Figure 11b shows the measured n-type capacitance values from the Vendor B second wafer. This wafer map shows four very distinct regions across the wafer. As may be seen, the capacitance values tend to decrease as viewed from left to right across a given row. The capacitance values also tend to decrease as one moves from the top of the wafer to the bottom of any given column.

Generally, it may be observed that the upper left portion of the wafer has higher capacitance values than the lower right portion of the wafer. From the looks of this wafer map, the wafer was probably sitting with what shows here as its sides on the top and bottom of the rack in the diffusion furnace.

Figure 12a shows the measured p-type capacitance values from the Vendor B first wafer. The N/A markings show the position of capacitors whose life was given to the voltage ramp stress test program development. This wafer map has some hints of regionalization of the capacitance values across the wafer. The fact that definitive regions do not show up for this data does not necessarily point to a problem. The measured values range from 23.49 pF to 24.63 pF, which shows only a single picoFarad range of values. What would show a possible problem would be if initial failures or low breakdown values existed on the wafer. Based on the capacitance measurement, there is not a definitive reason to believe the quality of the p-type capacitors is low.

			[illegible]	24.31			
	24.27	24.19	23.98	23.99	23.93	24.21	
	N/A	24.26	24.21	24.21	24.24	24.03	23.90
N/A	24.32	[illegible]	[illegible]	[illegible]	24.33	24.27	24.13
[illegible]	24.15	[illegible]	24.22	24.14	24.09	23.91	24.12
24.27	24.34	[illegible]	[illegible]	24.16	24.05	24.00	23.90
	24.24	[illegible]	24.14	24.13	N/A	23.94	23.86
	23.52	23.71	23.86	23.75	23.61	23.49	
			23.65	24.18			

Ranges

23.49-23.775	23.775-24.06	24.06-24.345	[illegible]

Figure 12a. Vendor B Wafer 1 P Capacitor Capacitance Wafer Map (pF).

			24.30	24.12			
	[illegible]	24.31	24.17	24.30	23.92	23.92	
	[illegible]	24.25	24.21	[illegible]	23.88	23.96	23.63
[illegible]	24.27	[illegible]	24.24	24.10	23.91	23.86	23.54
[illegible]	24.44	24.26	24.22	[illegible]	23.83	23.83	23.63
[illegible]	24.50	24.22	24.20	24.08	23.70	23.75	23.73
	24.34	24.15	24.08	23.93	23.85	23.67	23.84
	23.46	24.08	24.19	23.95	23.58	23.79	
			24.08	24.02			

Ranges

23.36-23.75	23.75-24.04	24.04-24.33	[illegible]

Figure 12b. Vendor B Wafer 2 P Capacitor Capacitance Wafer Map (pF).

Figure 12b shows the measured p-type capacitance values from the Vendor B second wafer. This

wafer map shows four somewhat defined regions of capacitance on the wafer. The higher capacitance values are generally found to be on the top and on the left side of the wafer. It is interesting to note that the p-type measured capacitance is not as well defined as the measured n-type capacitance. Of course, the choice of the bins has some play in this observation.

OXIDE THICKNESS

Table 10 is a breakdown of the mean oxide thickness values for the Vendor A tested oxides. The table contains both the censored and the uncensored numbers broken down by ramp rate and the type of capacitor. One may easily determine that the mean oxide thickness value for Vendor A is 191.70 Angstroms. The measured mean is about 35 Angstroms lower than the designed to oxide thickness of 225 Angstroms previously mentioned. For most of the ramp rates, the mean values of the N capacitors are higher than the overall mean and therefore the P capacitor values are lower than the vendor oxide thickness mean.

Table 10. Vendor A Mean Oxide Thickness Values (Angstroms).

	N		P		Total	
Rate	uncensored	censored	uncensored	censored	uncensored	censored
0.1	191.70	191.70	191.45	191.45	191.58	191.58
0.3	192.00	192.00	191.94	191.94	191.96	191.96
0.5	191.23	191.23	193.53	193.53	192.12	192.12
0.7	193.44	193.44	192.86	192.86	193.15	193.15
1.0	191.20	191.01	184.73	190.08	187.45	190.46
all	191.72	191.70	190.41	191.70	191.06	191.70

The histograms for the calculated oxide thickness for Vendor A may be found in Appendix E, Figure 41 through Figure 46. As one would expect, since the oxide thickness is based on the capacitance measurements, the populations appear to be normally distributed. The exceptions are, as was the case with the Vendor A capacitance, the uncensored total capacitor population and the uncensored p capacitor population. A low oxide thickness value exists, so that when the binning is performed, the other values get grouped in two bins.

Table 11 is a breakdown of the mean oxide thickness values for the Vendor B oxides tested. The table contains both the uncensored and censored measured values. The values are further broken down by the ramp rate, type of capacitor and the wafer on which the tested oxide resides. One may easily see that the mean oxide thickness for Vendor B is 225.12 Angstroms. The mean of the

measured oxide thickness is about 25 Angstroms lower than the designed oxide thickness of 250 Angstroms previously mentioned. For all ramp rates, the mean thickness values of the P capacitors are higher than the mean and therefore the N capacitor values are lower than the mean. If we compare wafer 1 against wafer 2, we see that wafer 1 has the higher mean for 2 of the ramp rates. Overall, the mean between the two wafers is different in the hundredths of Angstroms.

Table 11. Vendor B Mean Oxide Thickness Values (Angstroms).

uncensored									
Rate	N1	N2	N	P1	P2	P	W1	W2	Total
0.1	225.35	222.40	224.69	227.81	227.00	227.66	226.70	224.70	226.29
0.5	222.72	223.42	223.20	227.15	228.66	228.17	225.14	226.20	225.86
1.0	222.21	221.57	221.87	226.81	227.08	226.95	224.41	224.17	224.28
all	223.23	222.38	222.78	227.22	227.80	227.52	225.29	225.09	225.19

censored									
Rate	N1	N2	N	P1	P2	P	W1	W2	Total
0.1	224.43	224.40	223.92	227.81	227.00	227.66	226.41	224.70	226.04
0.5	222.14	223.42	223.05	227.15	228.66	228.17	225.00	226.20	225.83
1.0	222.21	221.57	221.81	226.81	227.08	226.95	224.41	224.17	224.28
all	222.79	222.38	222.57	227.22	227.80	227.52	225.15	225.09	225.12

The histograms for the calculated oxide thickness for Vendor B may be found in Appendix E, Figure 83 through Figure 100. For the most part, the populations appear to be normally distributed. The exception is that the n capacitor distributions have a tail on the right hand side of the histograms. Again, it should be noted that the censored capacitors for Vendor B were all n capacitors.

Figures 13a and 13b are wafer maps of the Vendor B n capacitors for the calculated oxide thickness of each structure. As before, the bolded data in Figure 13a represent the structures who were later censored from the data analysis. The locations marked N/A are those structures who were used for the test program development. For the most part, three regions of capacitance may be seen across the first Vendor B wafer, as seen in Figure 13a. Figure 13b, however, shows four distinct regions of capacitance across the wafer. As the oxide thickness is calculated from the measured capacitance, these wafer maps should look similar to the measured capacitance wafer maps. In general, the oxide thickness is thinnest along the left hand side of the wafer. The thicker oxides tend to show up on the right hand side of the wafer. Also note that the first Vendor B wafer was probably not sitting in the oxidation furnace at the same angle as the second wafer. This is noted because the thicker oxides tend to be on the bottom of wafer 1 and not the right hand side.

			N/A	N/A			
	N/A	N/A	234.1	224.0	224.3	222.2	
	N/A	N/A	221.7	222.1	220.6	223.7	225.2
223.2	220.3	218.4	219.1	220.0	220.7	N/A	222.6
217.1	220.4	218.0	221.5	222.5	223.3	221.8	222.9
231.1	220.7	218.6	220.0	222.4	223.3	223.9	225.0
	221.5	219.1	222.3	222.5	223.9	224.7	225.7
	228.5	226.9	225.8	227.0	227.9	229.0	
			227.6	222.3			

Ranges

217.1-221.35	221.35-225.6	225.6-229.85	229.85-234.1

Figure 13a. Vendor B Wafer 1 N Capacitor Oxide Thickness Wafer Map (Å).

			220.8	222.5			
	218.0	220.7	221.8	221.1	222.0	222.8	
	218.3	220.4	220.8	220.7	224.0	224.6	226.6
217.3	219.4	220.7	221.7	221.8	222.7	225.1	226.6
217.8	219.0	220.7	221.5	220.7	224.2	225.4	227.0
217.8	219.1	221.4	222.3	220.6	222.8	225.5	227.7
	220.9	221.0	221.0	223.0	224.9	225.8	225.2
	227.8	222.4	222.4	223.7	224.9	223.4	
			223.4	225.0			

Ranges

217.3-219.9	219.9-222.5	222.5-225.1	225.1-227.8

Figure 13b. Vendor B Wafer 2 N Capacitor Oxide Thickness Wafer Map (Å).

			225.1	225.5			
	225.8	226.6	228.6	228.5	229.0	226.4	
	N/A	225.9	226.4	226.4	226.1	228.1	229.3
N/A	225.4	223.3	223.8	224.7	225.3	225.8	227.1
224.8	227.0	222.5	226.3	227.0	227.5	229.2	227.2
225.9	225.2	223.4	224.1	226.9	227.9	228.4	229.3
	226.1	223.8	227.0	227.1	N/A	228.9	229.7
	233.0	231.2	229.7	230.8	232.1	233.3	
			231.8	228.2			

Ranges

222.5-225.2	225.2-227.9	227.9-230.6	230.6-233.3

Figure 14a. Vendor B Wafer 1 P Capacitor Oxide Thickness Wafer Map (Å).

Figures 14a and 14b are wafer maps of the Vendor B p capacitor wafer maps for the calculated oxide thickness of each structure. Figure 14a shows four regions of capacitance across, but they are not distinct as they circulate across the wafer. Figure 14b shows that the four capacitance regions across the wafer are more defined for the second Vendor B wafer. These wafer maps also

show that the oxide is thinnest along the left hand side and grows thicker the farther right one moves along the wafer. This is the same as was said about the n capacitors, as one would hope.

			225.6	227.2			
	223.3	225.5	228.6	225.6	229.1	229.1	
	224.3	226.0	226.4	225.2	229.5	228.8	[illegible]
226.6	225.8	225.2	226.1	227.4	229.2	229.7	232.8
223.0	224.3	225.9	226.3	225.1	230.0	230.0	232.0
223.2	223.7	226.3	226.5	227.6	[illegible]	230.8	231.0
	225.2	227.0	227.6	229.0	229.8	231.0	229.9
	231.6	227.6	226.6	228.9	[illegible]	230.4	
			227.6	228.2			

Ranges

223.0-225.6	225.6-228.3	228.3-230.9	230.9-233.6

Figure 14b. Vendor B Wafer 2 P Capacitor Oxide Thickness Wafer Map (Å).

BREAKDOWN DATA

This section will discuss the data from the voltage ramp stress procedure. Specifically, the measured pre-stress current, the measured breakdown voltage and the calculated breakdown field will be discussed.

PRE-STRESS CURRENT

The measured pre-stress currents showed great variability in their ranges. For this reason, little analysis was performed on this data. As with the other data measured and calculated, we were looking at various parameters which could potentially be used for process control as a predictor of a poor quality oxide. The wide range of measured initial currents, however, quickly put to rest the use of this as a possible process control parameter.

The histograms for the measured pre-stress current may be found in Appendix E. The pre-stress histograms for Vendor A are found in Figure 47 through Figure 52, while the histograms for Vendor B are found in Figure 101 through Figure 118. Because of the wide range of measured values for Vendor A, the methodology used to bin the data does not allow much information to be gained. A different method of binning the data or further censoring of data may have yielded a

more useful distribution, but it is doubtful. The Vendor B data, on the other hand, does not show the wide range of values. Therefore, the bin values are smaller and the data is more evenly distributed between the bins. These histograms appear to show normally distributed populations.

Figures 15a, 15b, 16a and 16b are wafer maps for the pre-stress currents measured for each of the Vendor B structures. These wafer maps were prepared in the hopes that some indication of lack of quality may be gleaned from the simple current measurement. As may be seen in the wafer maps, however, there is no evidence of correlation between the measured currents and failure.

			N/A	N/A			
	N/A	N/A	**840.1**	248.1	300.8	453.5	
	N/A	N/A	117.3	657.9	[illegible]	706.7	530.0
[illegible]	285.9	292.0	531.4	354.6	444.3	N/A	455.7
549.3	144.9	579.9	681.5	[illegible]	[illegible]	561.2	558.0
379.2	425.5	160.0	160.3	432.0	303.5	92.5	639.0
	374.7	576.9	[illegible]	[illegible]	670.0	189.5	[illegible]
	865.1	864.3	1215.0	[illegible]	**554.0**	789.9	
			827.8	145.6			

Ranges

92.5-397.6	397.6-702.8	702.8-1007.9	[illegible]

Figure 15a. Vendor B Wafer 1 N Capacitor Pre-Stress Current Wafer Map (pA).

			[illegible]	822.5			
	153.0	439.0	[illegible]	642.5	1177.0	[illegible]	
	[illegible]	345.0	837.5	960.0	166.0	129.5	122.0
600.5	110.0	341.5	125.0	841.0	149.5	[illegible]	318.5
676.5	798.5	682.5	918.5	[illegible]	777.5	147.5	699.5
1135.0	1316.0	920.0	[illegible]	657.0	[illegible]	154.5	871.0
	453.5	[illegible]	645.5	889.0	[illegible]	798.5	760.5
	[illegible]	1143.0	1138.0	[illegible]	672.0	628.5	
			1048.0	917.0			

Ranges

110.0-484.5	484.5-859.0	859.0-1233.5	[illegible]

Figure 15b. Vendor B Wafer 2 N Capacitor Pre-Stress Current Wafer Map (pA).

			35.0	606.2			
	800.5	627.4	796.5	460.7	666.0	341.8	
	N/A	668.8	145.7	546.7	1059.0	169.0	671.7
N/A	539.3	452.7	422.8	531.5	410.5	153.7	526.3
500.8	336.1	202.8	1022.0	[illegible]	760.0	1247.0	142.5
800.5	194.4	250.7	226.5	676.5	[illegible]	705.0	1001.0
	467.4	361.8	221.5	459.0	N/A	1223.0	750.0
	836.7	846.0	1253.0	543.6	752.9	737.5	
			741.7	171.5			

Ranges

35.0-339.5	339.5-644.0	644.0-948.5	948.5-1253.0

Figure 16a. Vendor B Wafer 1 P Capacitor Pre-Stress Current Wafer Map (pA).

			531.5	419.0			
	1355.0	87.5	803.0	339.5	1512.0	476.5	
	621.5	1360.0	1082.0	448.0	136.5	35.0	729.0
1083.0	469.0	895.0	11.1	1412.0	1045.0	1063.0	1286.0
542.5	1370.0	1042.0	925.5	1084.0	1494.0	1016.0	80.0
1121.0	728.5	1384.0	749.5	1046.0	55.0	1367.0	1332.0
	1178.0	298.0	779.0	45.5	156.5	911.0	506.0
	188.0	773.5	258.5	733.5	1111.0	1238.0	
			953.5	599.5			

Ranges

11.1-386.3	386.3-761.5	761.5-1136.7	1136.7-1512.0

Figure 16b. Vendor B Wafer 2 P Capacitor Pre-Stress Current Wafer Map (pA).

BREAKDOWN VOLTAGE

Table 12 is a listing of the mean breakdown voltage values for the Vendor A tested oxides. The table contains both the censored and the uncensored numbers broken down by ramp rate and the type of capacitor. One may easily determine that the mean breakdown voltage for Vendor A is 26.04 volts. For the most part, the mean n capacitor breakdown voltage is lower than the mean p capacitor breakdown voltage.

Table 12. Vendor A Mean Breakdown Voltage Values (V).

Rate	N		P		Total	
	uncensored	censored	uncensored	censored	uncensored	censored
0.1	25.78	25.78	24.90	24.90	25.35	25.35
0.3	26.55	26.55	26.35	26.35	26.42	26.42
0.5	26.59	26.59	26.76	26.76	26.66	26.66
0.7	26.58	26.58	27.29	27.29	26.94	26.94
1.0	23.98	26.30	26.11	25.84	25.21	26.03
all	25.81	26.22	25.93	25.87	25.87	26.04

The histograms for the Vendor A measured breakdown voltage may be found in Appendix E, Figure 53 through Figure 58. The p capacitor population appears to be normally distributed. The total population and n capacitor population also appear to be normally distributed, however, they also show a tail on the left side (lower voltage). It is interesting to note that even though the n capacitor population has this early tail, the lowest voltage for this population is actually higher than the lowest p capacitor voltage. Also, as shown in Table 12, the mean breakdown voltage for the censored n capacitor population is higher than the mean breakdown voltage for the censored p capacitor population.

Table 13 is a listing of the mean breakdown voltage values for the Vendor B oxides tested. The table contains both the uncensored and censored measured values. The values are further broken down by the ramp rate, type of capacitor and the wafer on which the tested oxide resides. One may easily see that the mean breakdown voltage for Vendor B is 29.08 volts. For the most part, the n capacitor mean breakdown voltage is lower than the p capacitor mean breakdown voltage.

Table 13. Vendor B Mean Breakdown Voltage Values (V).

uncensored									
Rate	N1	N2	N	P1	P2	P	W1	W2	Total
0.1	30.33	29.92	30.21	28.15	29.11	28.33	29.12	29.15	29.20
0.5	31.09	29.40	29.93	30.01	29.44	29.62	30.50	29.42	29.76
1.0	28.89	28.16	28.49	29.50	29.33	29.41	29.18	28.71	28.93
all	29.76	28.79	29.25	29.17	29.36	29.27	29.45	29.08	29.26

censored									
Rate	N1	N2	N	P1	P2	P	W1	W2	Total
0.1	28.52	29.92	28.87	28.15	29.11	28.33	28.30	29.51	28.56
0.5	29.99	29.40	29.57	30.01	29.44	29.62	30.00	29.42	29.60
1.0	28.89	28.16	29.49	29.50	29.33	29.41	29.18	28.71	28.93
all	29.01	28.76	28.89	29.17	29.36	29.27	29.09	29.08	29.08

The histograms for the Vendor B measured breakdown voltage may be found in Appendix E, The

histograms for this data appear in Appendix E, Figure 119 through Figure 136. For the most part, these histograms appear to show a bi-modal distribution. Most of the breakdown histograms for Vendor B show a normally distributed population in the upper twenty volt range. There also exists a small percentage of the population in the lower twenty volt range. This is more than just an early tail on the normal distribution. It is more of oxides which may cause a late life reliability concern.

Figure 17a, Figure 17b, and Figure 17c are wafer maps for the Vendor B n capacitor breakdown voltages. Figure 17a is the first wafer n capacitors. There are areas for each of the bins on the wafer, but they are not distinct.

			N/A	N/A			
	N/A	N/A	[illegible]	29.12	29.16	30.67	
	N/A	N/A	30.15	28.87	18.31	29.08	29.28
29.36	28.64	28.39	28.48	29.70	28.69	N/A	30.05
28.22	28.65	29.43	28.79	28.93	29.03	28.83	28.98
18.72	28.69	29.51	31.03	28.91	29.04	30.45	30.38
	28.80	29.58	30.01	28.93	29.11	30.34	30.38
	30.85	30.86	30.72	29.74	[illegible]	30.92	
			[illegible]	31.35			

Ranges

18.31-23.99	23.99-29.67	29.67-35.33	[illegible]

Figure 17a. Vendor B Wafer 1 N Capacitor Breakdown Voltage Wafer Map (V).

Figure 17b is the first wafer n capacitors with the censored values not included in the bin determination process. It is interesting to note that when binned this way, all the breakdown voltages, but the early failures, are lumped into the highest bin.

			N/A	N/A			
	N/A	N/A	**40.98**	[illegible]	[illegible]	[illegible]	
	N/A	N/A	[illegible]	[illegible]	18.31	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	N/A	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
18.72	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	**41.02**	[illegible]	
			40.98	[illegible]			

Ranges

18.31-21.57	21.57-24.83	24.83-28.09	[illegible]

Figure 17b. Vendor B Wafer 1 N Capacitor Breakdown Voltage Wafer Map (V).

Figure 17c is the n capacitors on the second wafer. This wafer shows some partitioning of breakdown voltage across the wafer. For example, right and upper n capacitors tend to be binned into the highest category, while left and lower tend to be binned into the second highest category. But it is still not as distinct as say the capacitance was.

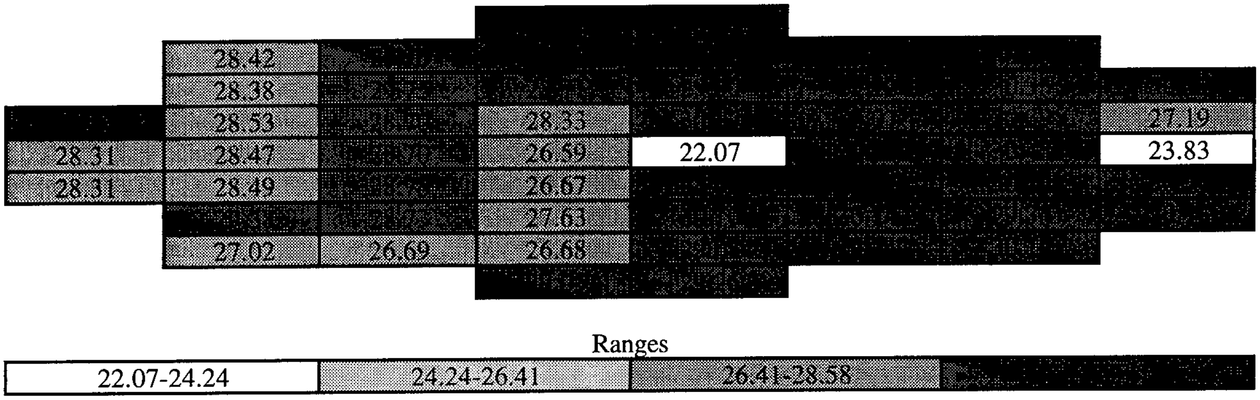

Figure 17c. Vendor B Wafer 2 N Capacitor Breakdown Voltage Wafer Map (V).

Figure 18a and Figure 18b are wafer maps of the p capacitors for the two Vendor B wafers. Not much information is able to be gathered from either wafer map. It is interesting to note that on the first wafer, Figure 18a, most of the p capacitors are binned in the second highest bin, while on the second wafer, Figure 18b, most of the capacitors are grouped into the highest bin.

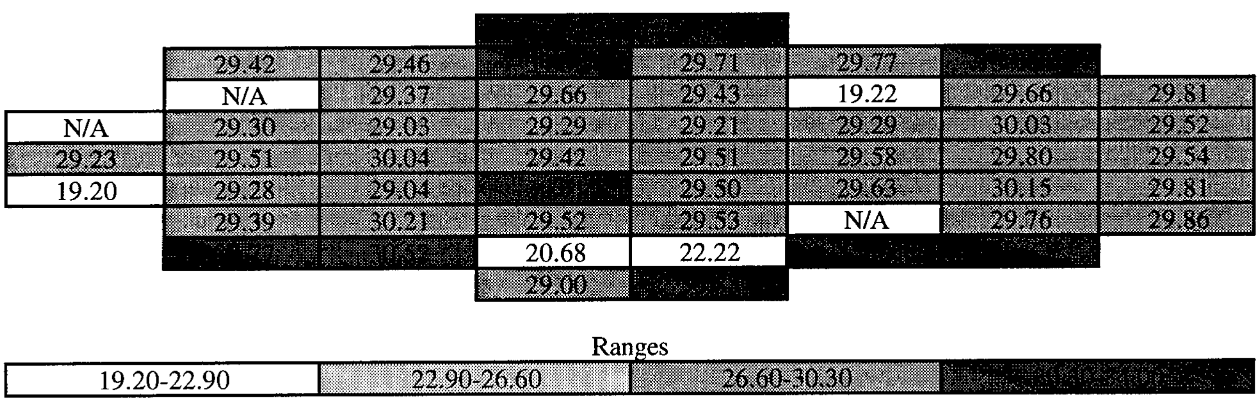

Figure 18a. Vendor B Wafer 1 P Capacitor Breakdown Voltage Wafer Map (V).

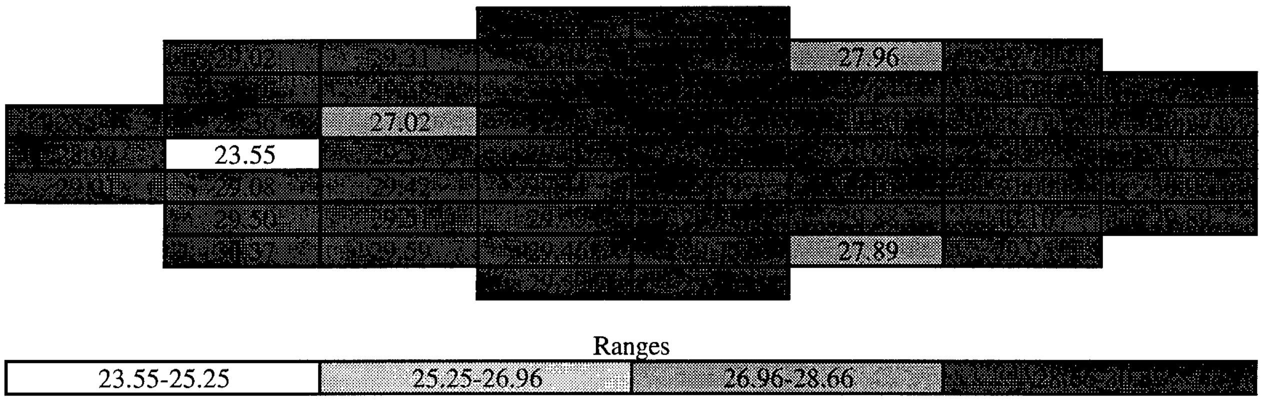

Figure 18b. Vendor B Wafer 2 P Capacitor Breakdown Voltage Wafer Map (V).

BREAKDOWN FIELD

Table 14 is a listing of the mean breakdown field values for the Vendor A tested oxides. The table contains both the censored and the uncensored numbers broken down by ramp rate and the type of capacitor. One may easily determine that the mean breakdown field for Vendor A is 13.57 MV/cm. For the most part, the n capacitor mean breakdown field is higher than the p capacitor mean breakdown field.

Table 14. Vendor A Mean Breakdown Field Values (MV/cm).

	N		P		Total	
Rate	uncensored	censored	uncensored	censored	uncensored	censored
0.1	13.32	13.32	12.99	12.99	13.16	13.16
0.3	13.83	13.83	13.73	13.73	13.76	13.76
0.5	13.91	13.91	13.93	13.93	13.92	13.92
0.7	13.74	13.74	14.16	14.16	13.95	13.95
1.0	12.55	13.77	14.36	13.60	13.60	13.67
all	13.42	13.63	13.69	13.51	13.55	13.57

The histograms for the calculated breakdown field of Vendor A may be found in Appendix E, Figure 59 through Figure 67. For the most part, the histograms of the breakdown field for Vendor A appear to be bi-modally distributed. Most of the data appears normally distributed around 13.7 MV/cm, however, another distinct grouping of the data which appears to be more than just an extended tail of the distribution exists around 11.5 MV/cm. This grouping of early breakdown fields show up as mid to late life oxide reliability problems.

Table 15 is a listing of the mean breakdown field values for the Vendor B oxides tested. The table contains both the uncensored and censored measured values. The values are further broken down by the ramp rate, type of capacitor and the wafer on which the tested oxide resides. One may easily see that the mean breakdown field for Vendor B is 12.93 MV/cm. For the most part, the n capacitor mean breakdown fields are higher than that of the p capacitors.

Table 15. Vendor B Mean Breakdown Field Values (MV/cm).

uncensored									
Rate	N1	N2	N	P1	P2	P	W1	W2	Total
0.1	13.44	13.40	13.43	12.42	12.83	12.49	12.88	13.11	12.92
0.5	13.95	13.16	13.41	13.21	12.88	12.99	13.55	13.01	13.18
1.0	13.00	12.71	12.85	13.00	12.92	12.96	13.00	12.81	12.90
all	13.32	12.95	13.12	12.85	12.89	12.87	13.08	12.92	13.00

censored									
Rate	N1	N2	N	P1	P2	P	W1	W2	Total
0.1	12.71	13.40	12.89	12.42	12.83	12.49	12.54	13.11	12.66
0.5	13.50	13.16	13.26	13.21	12.88	12.99	13.33	13.01	13.11
1.0	13.00	12.71	12.85	13.00	12.92	12.96	13.00	12.81	12.90
all	13.02	12.95	12.98	12.85	12.89	12.87	12.93	12.92	12.93

The histograms for the calculated breakdown field of Vendor B may be found in Appendix E, Figure 137 through Figure 154. These histograms show what appears to be a bi-modal distribution of the breakdown field data. A large percentage of the data appears to be normally distributed around 12.5 MV/cm. The other small percentage of data is scattered in the 8 to 10 MV/cm range. It is these data points who cause concern for the early breakdown of the oxides. It is likely that these oxides will cause mid to late life oxide problems.

The wafer maps for the Vendor B breakdown field data are in the following figures. The data was looked at in several ways. First, as with the breakdown voltage, the n capacitors have a wafer map for the wafer 1 n capacitor data, the wafer 1 n capacitor censored data and the wafer 2 n capacitor data. The p capacitor data is only charted as wafer 1 or wafer 2 as with the breakdown voltage data. The other way the data has been plotted relates to how the breakdown field has been calculated. In our data analysis, we calculated the breakdown field by using the actual breakdown voltage and the calculated oxide thickness based on the measured capacitance. This data is called *Actual* in the following wafer maps. In a production environment, the usual way to compute the breakdown field would be by using the measured breakdown voltage and the designed to oxide thickness. This data is called *Generic* in the following wafer maps.

Figure 19a, Figure 19b and Figure 19c are wafer maps of the n capacitors breakdown field based on the measured breakdown voltage and the calculated oxide thickness. From Figure 19a, one may say that the n capacitor data for wafer 1 at the top of the wafer tends to the second lowest bin, while the bottom of the wafer tends to the second highest bin. In general, however, there is not a clear distinction between breakdown field levels across the wafer. It is interesting to note that by censoring out the data, as seen in Figure 19b, almost all of the data is grouped into the highest bin. Finally, Figure 19c shows the n capacitor data for the second wafer from Vendor B. The majority of the data is grouped into the highest bin, but it should be noted that several low field breakdowns do exist on this wafer.

			N/A	N/A			
	N/A	N/A	[illegible]	13.0	13.0	13.8	
	N/A	N/A	13.6	13.0	8.3	13.0	13.0
13.2	13.0	13.0	13.0	13.5	13.0	N/A	13.5
13.0	13.0	13.5	13.0	13.0	13.0	13.0	13.0
8.1	13.0	13.5	14.1	13.0	13.0	13.6	13.5
	13.0	13.5	13.5	13.0	13.0	13.5	13.0
	13.5	13.6	13.6	13.1	[illegible]	13.5	
			[illegible]	14.1			

Ranges

8.1-10.6	10.6-13.1	13.1-15.5	15.5-18.0

Figure 19a. Vendor B Wafer 1 N Capacitor Actual Breakdown Field Wafer Map (MV/cm).

			N/A	N/A			
	N/A	N/A	17.51	[illegible]	[illegible]	[illegible]	
	N/A	N/A	[illegible]	[illegible]	8.3	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	N/A	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
8.1	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	18.0	[illegible]	
			18.0	[illegible]			

Ranges

8.1-9.6	9.6-11.1	11.1-12.6	12.6-14.1

Figure 19b. Vendor B Wafer 1 N Capacitor Actual Breakdown Field Wafer Map (MV/cm).

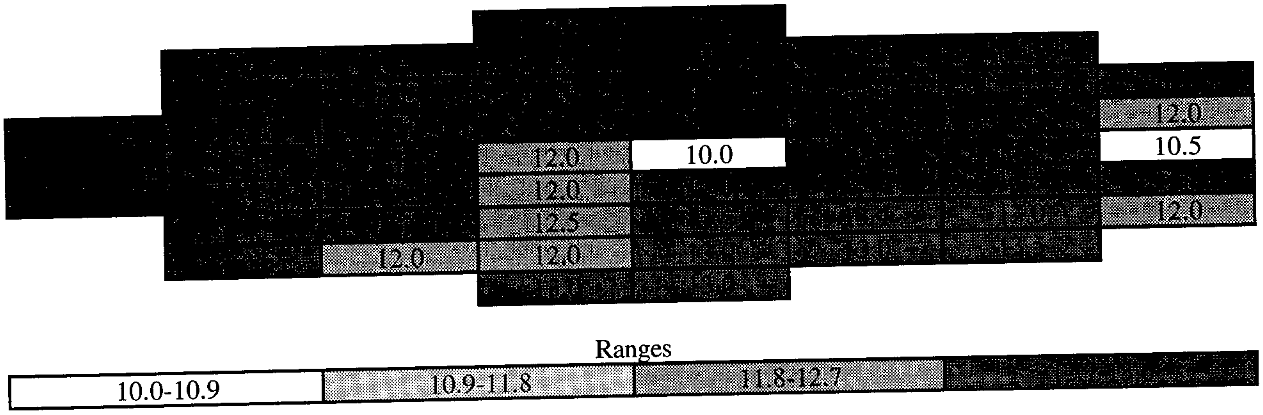

Figure 19c. Vendor B Wafer 2 N Capacitor Actual Breakdown Field Wafer Map (MV/cm).

Figure 20a, Figure 20b and Figure 20c are wafer maps of the n capacitors breakdown field based on the measured breakdown voltage and the design to oxide thickness. From Figure 20a, one may say that the n capacitor data for wafer 1 at the top of the wafer tends to the second lowest bin, while the bottom of the wafer tends to the second highest bin. In general, however, there is not a clear distinction between breakdown field levels across the wafer. It is interesting to note that by censoring out the data, as seen in Figure 20b, almost all of the data is grouped into the highest bin. For the first Vendor B wafer, the method for calculating the breakdown field has made little difference as the wafer maps are almost identical. Figure 20c, however, shows the n capacitor data for the second wafer from Vendor B. While a large percentage of the data is still grouped into the highest bin, several more of the tested locations are now grouped into lower breakdown field bins. As before, it should be noted that several low field breakdowns do exist on this wafer.

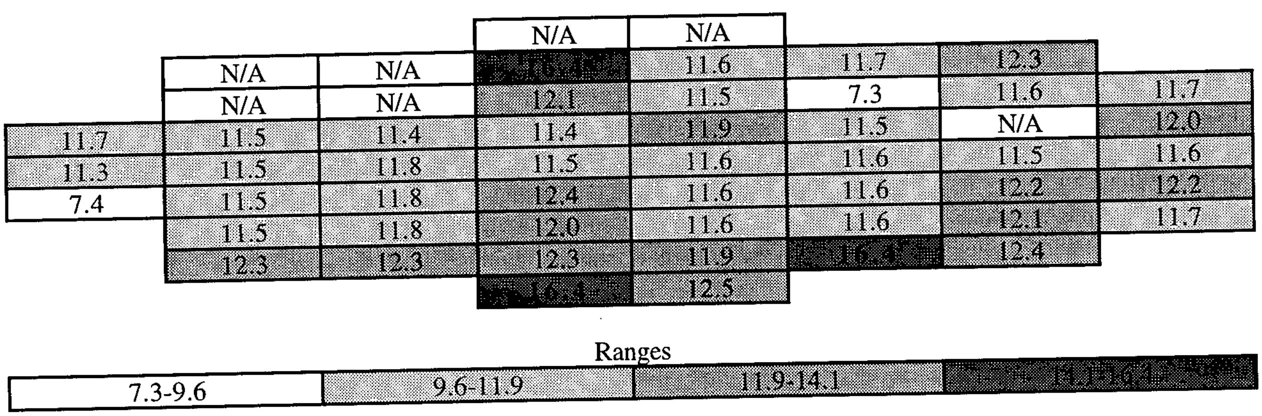

Figure 20a. Vendor B Wafer 1 N Capacitor Generic Breakdown Field Wafer Map (MV/cm).

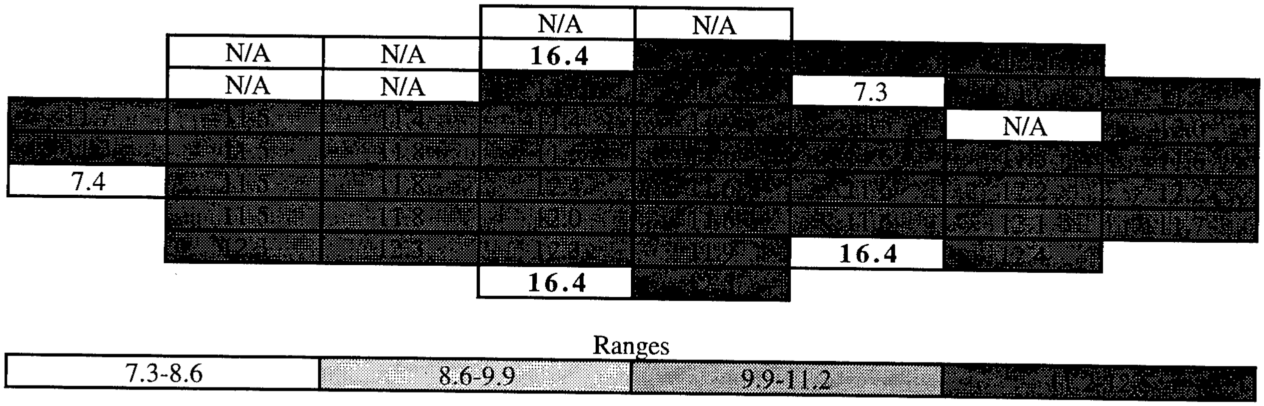

Figure 20b. Vendor B Wafer 1 N Capacitor Generic Breakdown Field Wafer Map (MV/cm).

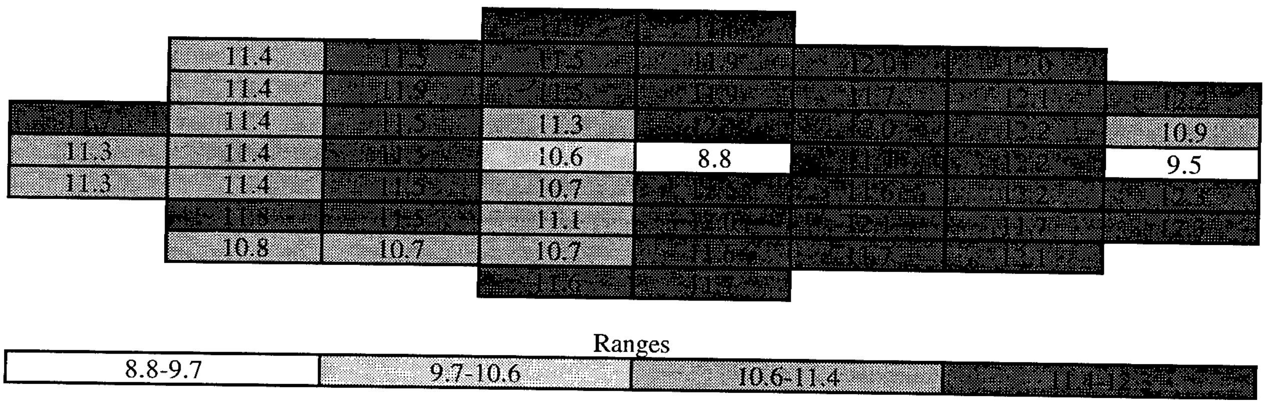

Figure 20c. Vendor B Wafer 2 N Capacitor Generic Breakdown Field Wafer Map (MV/cm).

Figure 21a and Figure 21b are wafer maps of the breakdown field as calculated from the measured breakdown voltage and the calculated oxide thickness. Several low field failures are noted in Figure 21a. The majority of the breakdowns are grouped into the second highest bin, but no distinct regions of breakdown field appear across the wafer. In Figure 21b, the majority of the p capacitors are grouped into the highest bin.

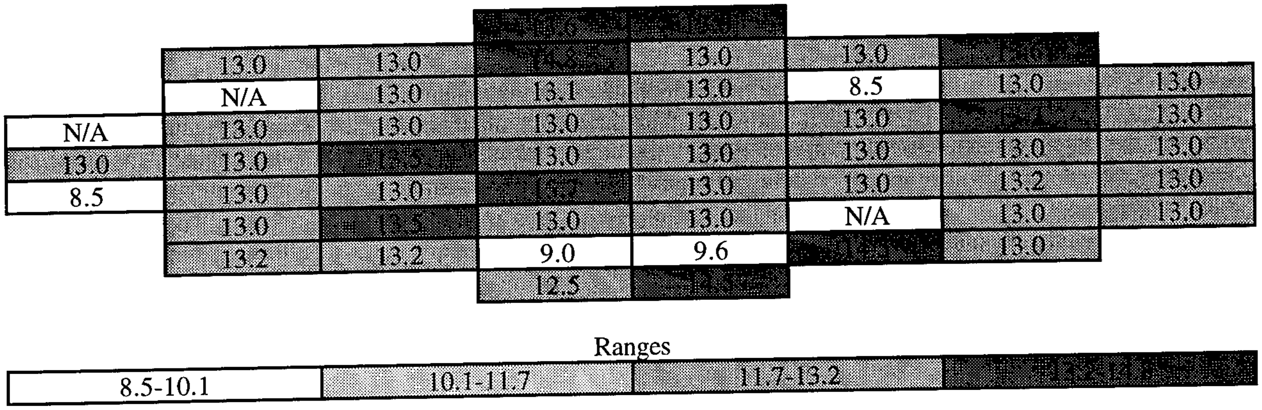

Figure 21a. Vendor B Wafer 1 P Capacitor Actual Breakdown Field Wafer Map (MV/cm).

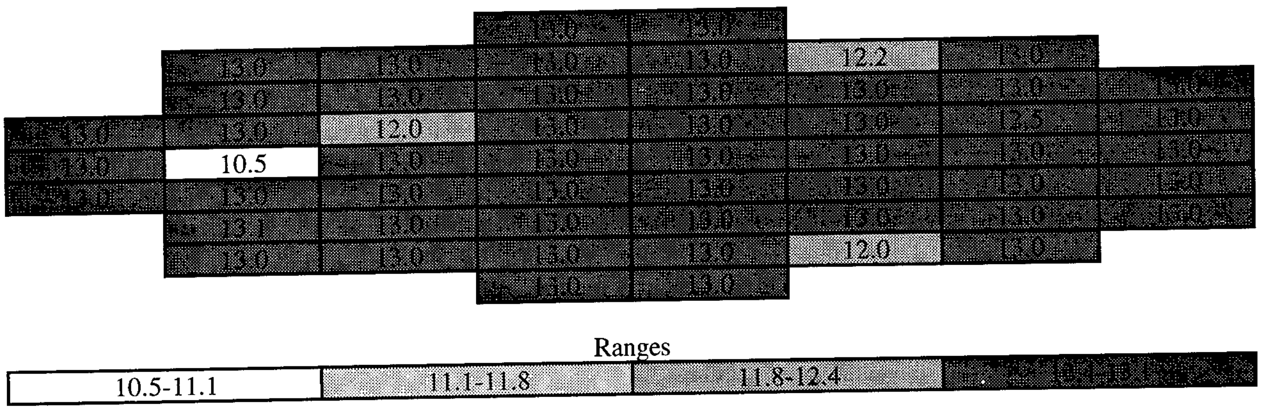

Figure 21b. Vendor B Wafer 2 P Capacitor Actual Breakdown Field Wafer Map (MV/cm).

Figure 22a and Figure 22b are wafer maps of the breakdown field as calculated from the measured breakdown voltage and the as designed oxide thickness.

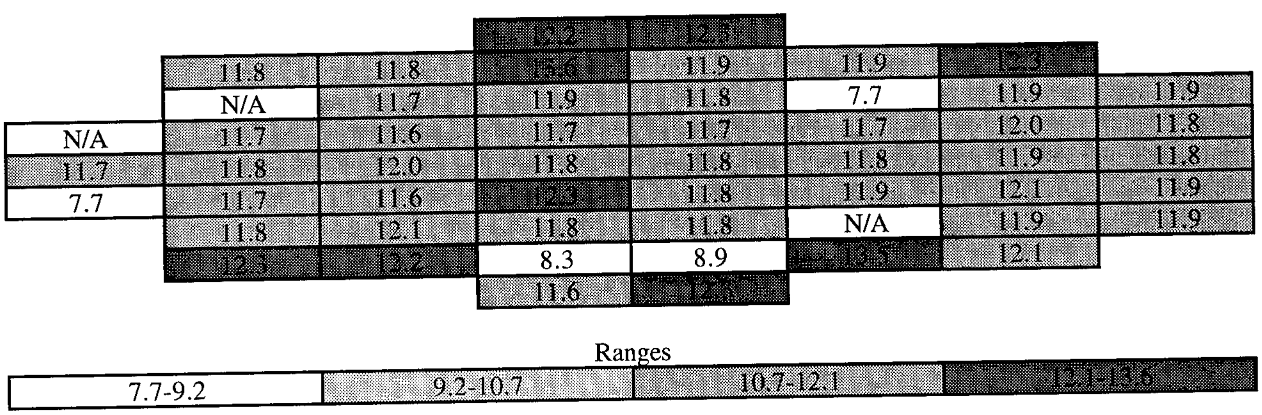

Figure 22a. Vendor B Wafer 1 P Capacitor Generic Breakdown Field Wafer Map (MV/cm).

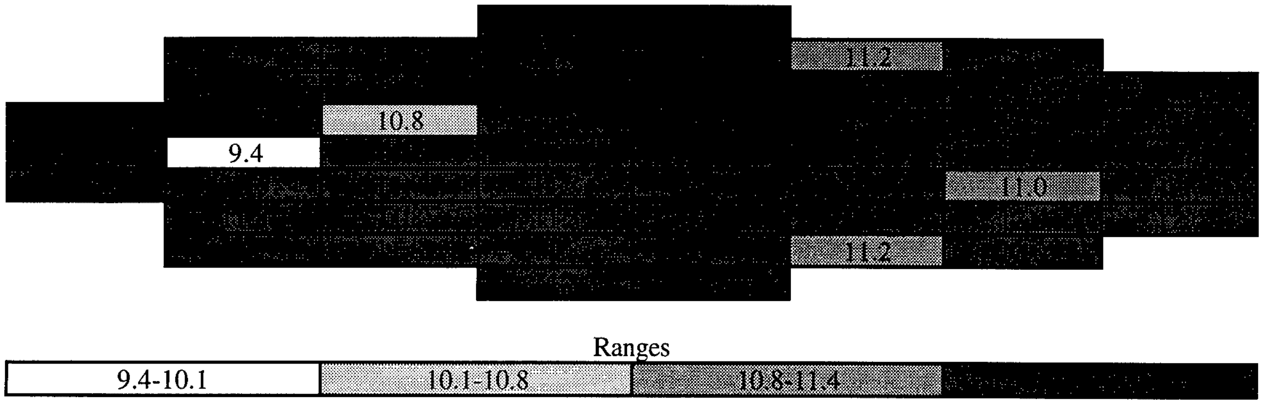

Figure 22b. Vendor B Wafer 2 P Capacitor Generic Breakdown Field Wafer Map (MV/cm).

Although the wafer maps did not yield any stand out information, they are a useful visual tool for analysis of wafer collected data. Changes could have been made to the wafer map analysis, such as increasing the number of bins used and using consistent bins across all wafer maps of a parameter to see if that changed the usefulness of the data. However, this was not felt necessary because of the multitude of other data analysis techniques utilized.

CUMULATIVE BREAKDOWN DISTRIBUTIONS

Figures 23 through 27 are cumulative breakdown curves for the n capacitor, p capacitor and total sample populations for Vendor A and Vendor B. These plots provide an overview of the cumulative breakdown distributions for the data based on the type of the capacitor, the vendor of the capacitor, and the wafer on which the capacitor resides. Appendix F, Figure 155 through Figure 182, contain more cumulative breakdown curves for the data analyzed at lower levels, such as the Vendor A n capacitor population by ramp rate. The cumulative breakdown curve is a simple plot where the y-axis is the percentage of devices which have broken down, out of all the devices tested, at the particular electric field along the x-axis. Therefore, the minimum y-axis value is 0 percent and the maximum value is 100 percent. The x-axis of these curves varies from curve to curve, as the minimum value is the first field at which a breakdown occurs and the maximum value is the last field at which a breakdown occurs. By plotting the failure data this way, one is able to visually note any areas for concern. Some traits of a cumulative breakdown curve which are cause for concern are a high percentage of failed devices at low fields and knees in the curve. These both are signals that mid to late life oxide reliability may be experienced.

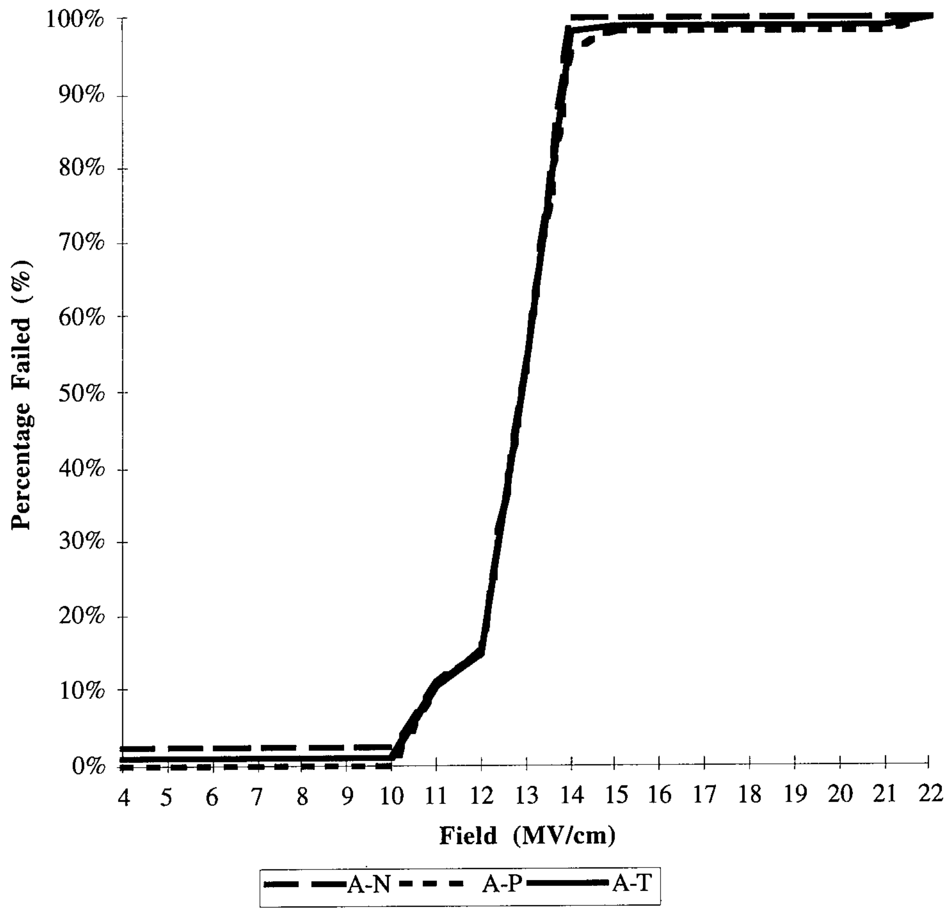

Figure 23. Uncensored Vendor A cumulative breakdown curve for n, p and all capacitor data.

Figure 23 provides a view of the cumulative breakdown of the Vendor A data grouped as the uncensored total population (A-T), uncensored n capacitors (A-N) and the uncensored p capacitors (A-P). There is a single low field breakdown at 4 MV/cm of an n capacitor. The rest of the population begins to experience breakdown at 11 MV/cm, with the majority of the breakdowns occurring at 13 MV/cm and 14 MV/cm. This is the intrinsic population. It is interesting to note the knee of the curve. Almost 20% of the population is accounted for with the fields below the knee.

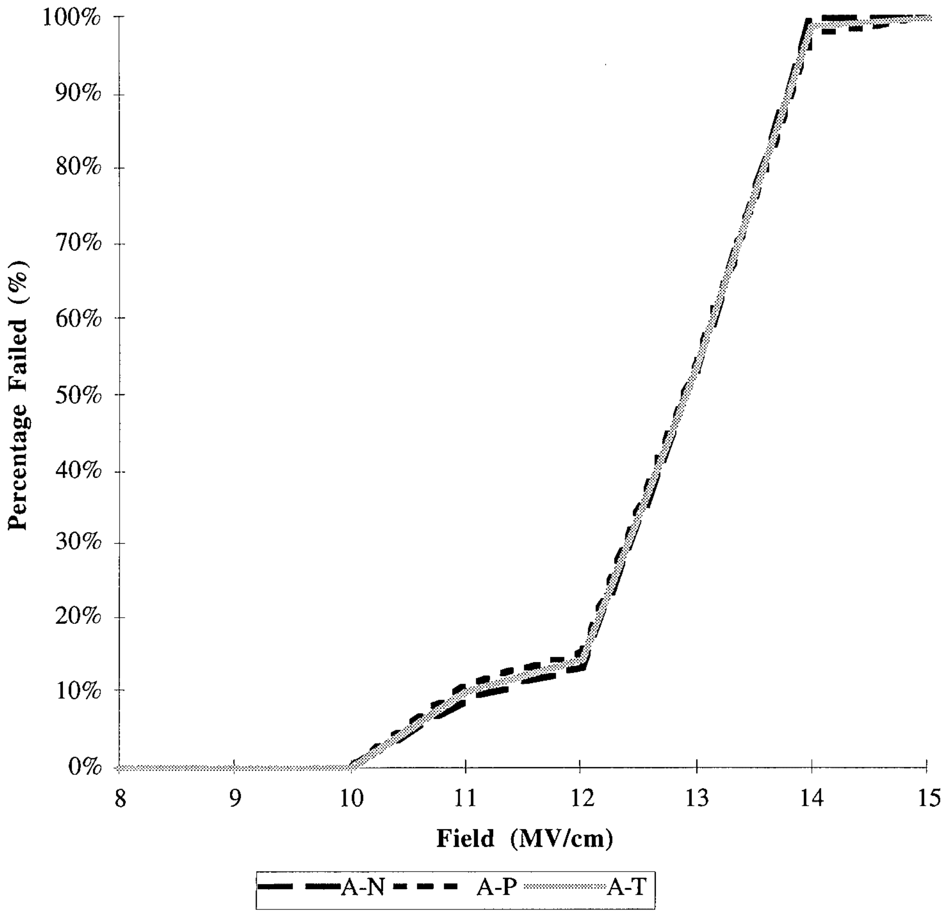

Figure 24. Censored Vendor A cumulative breakdown curve for n, p and all capacitor data.

Figure 24 is a view of the censored cumulative distribution curve for the Vendor A data. With the censoring, the first breakdowns occur at 11 MV/cm field across the oxide.

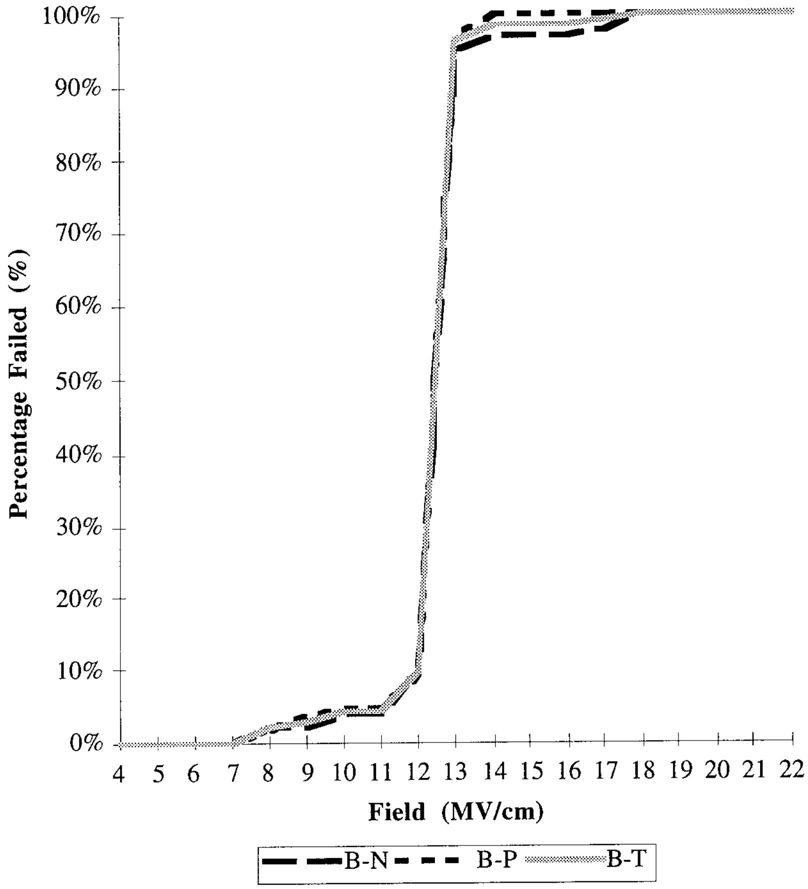

Figure 25. Uncensored Vendor B cumulative breakdown curve for n, p and all capacitor data.

Figure 25 provides a view of the cumulative breakdown of the Vendor B data grouped as the uncensored total population (B-T), uncensored n capacitors (B-N) and the uncensored p capacitors (B-P). The initial breakdown of the Vendor B oxides occurs at 8 MV/cm. A few more scattered breakdowns occur through a field of 12 MV/cm. The bulk of the Vendor B oxides breakdown at a field of 13 MV/cm. For Vendor B, approximately 10% of the population has broken down at the knee of the curve. The main portion of the intrinsic population is then reached at the 13 MV/cm field.

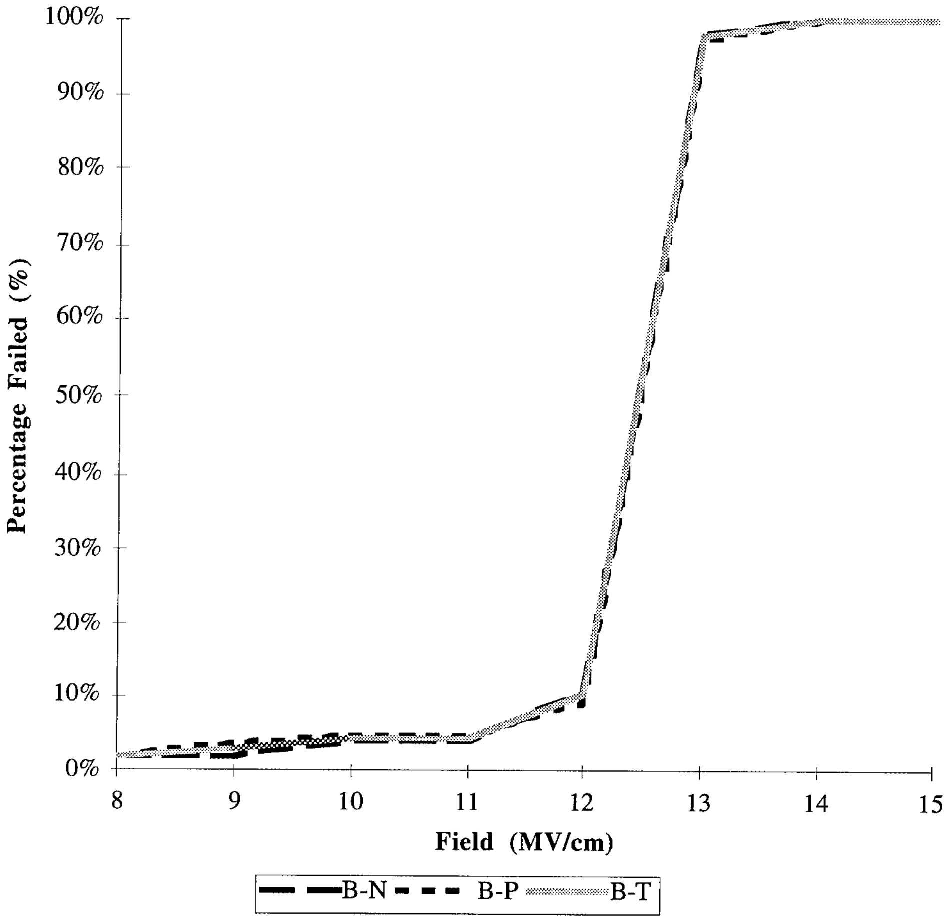

Figure 26. Censored Vendor B cumulative breakdown curve for n, p and all capacitor data.

Figure 26 provides a view of the censored cumulative breakdown distribution. It is interesting to note that the data which has been censored were all high field failures.

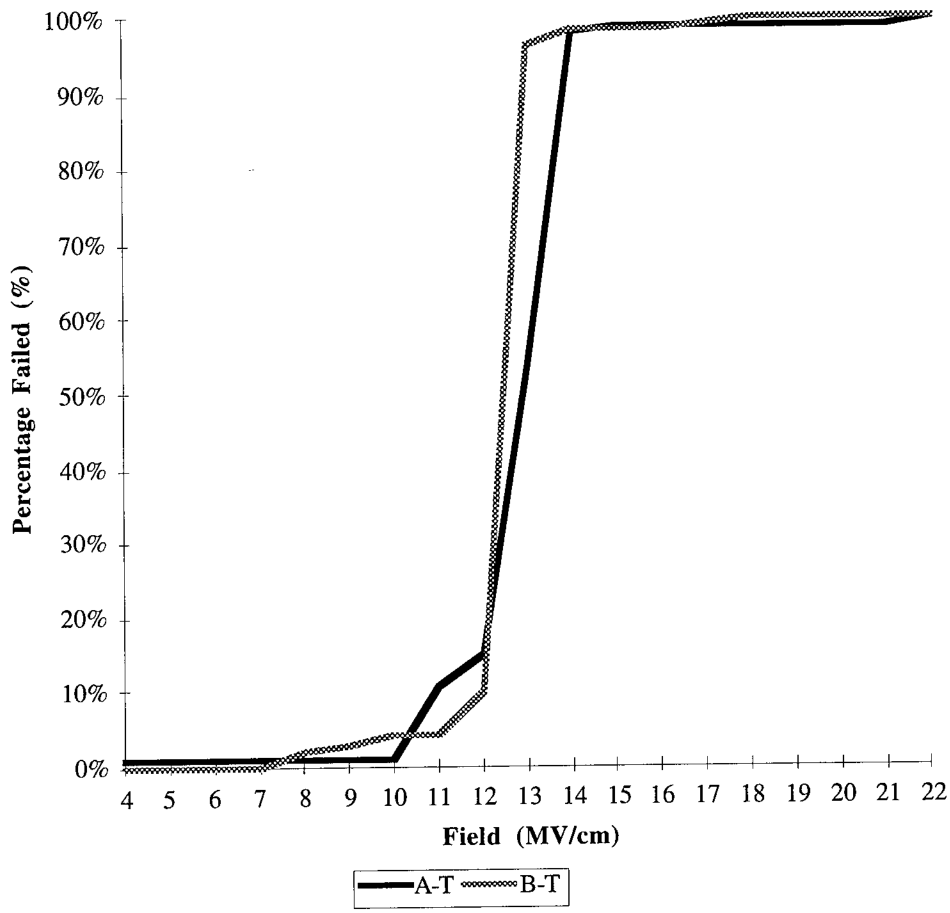

Figure 27. Uncensored Vendor A versus Vendor B cumulative breakdown curve for all capacitor data.

Figure 27 is the uncensored cumulative breakdown curve for all of the Vendor A and Vendor B capacitor data. It is interesting to note that both vendors' oxides start into intrinsic breakdown around 12 MV/cm. The knee for Vendor starts at a higher field than Vendor B, however, the 'early' failures increase more rapidly than for Vendor B. It is also interesting to note that the first failure is for Vendor A is at 4 MV/cm and the next failure does not occur until 11 MV/cm, while the first Vendor B failure does not occur until 8 MV/cm.

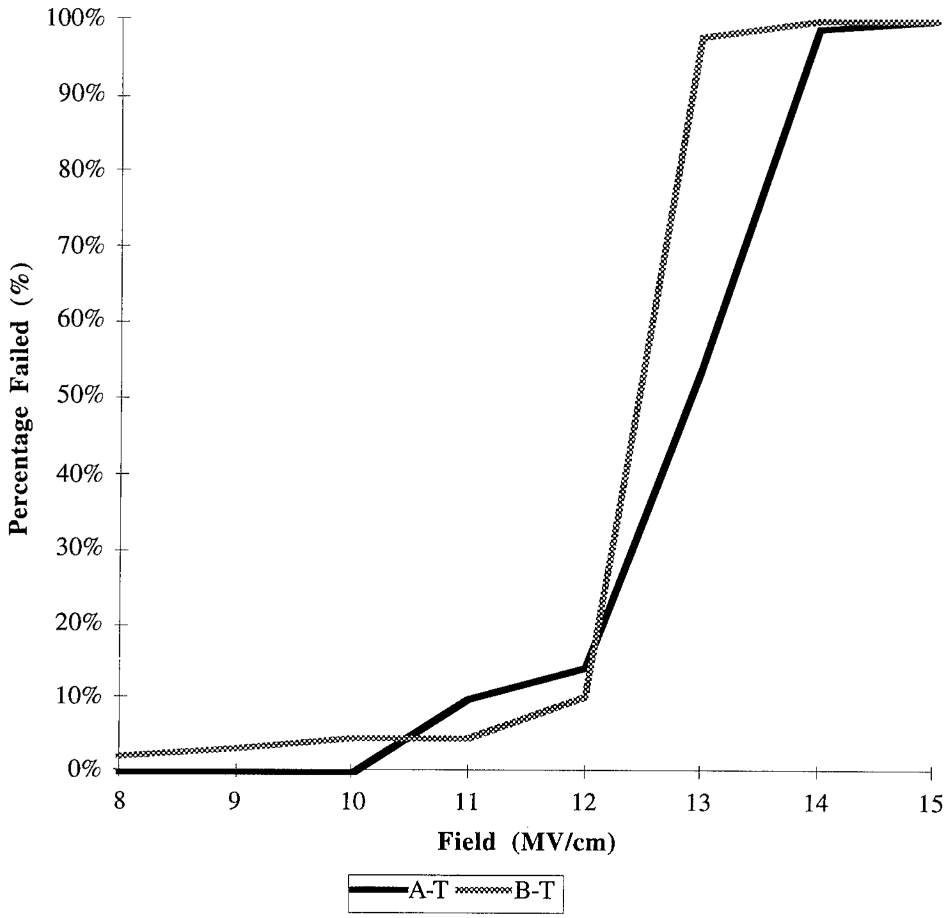

Figure 28. Censored Vendor A versus Vendor B cumulative breakdown curve for all capacitor data.

The censored cumulative breakdown data for all of the capacitors of Vendor A and Vendor B is shown in Figure 28.

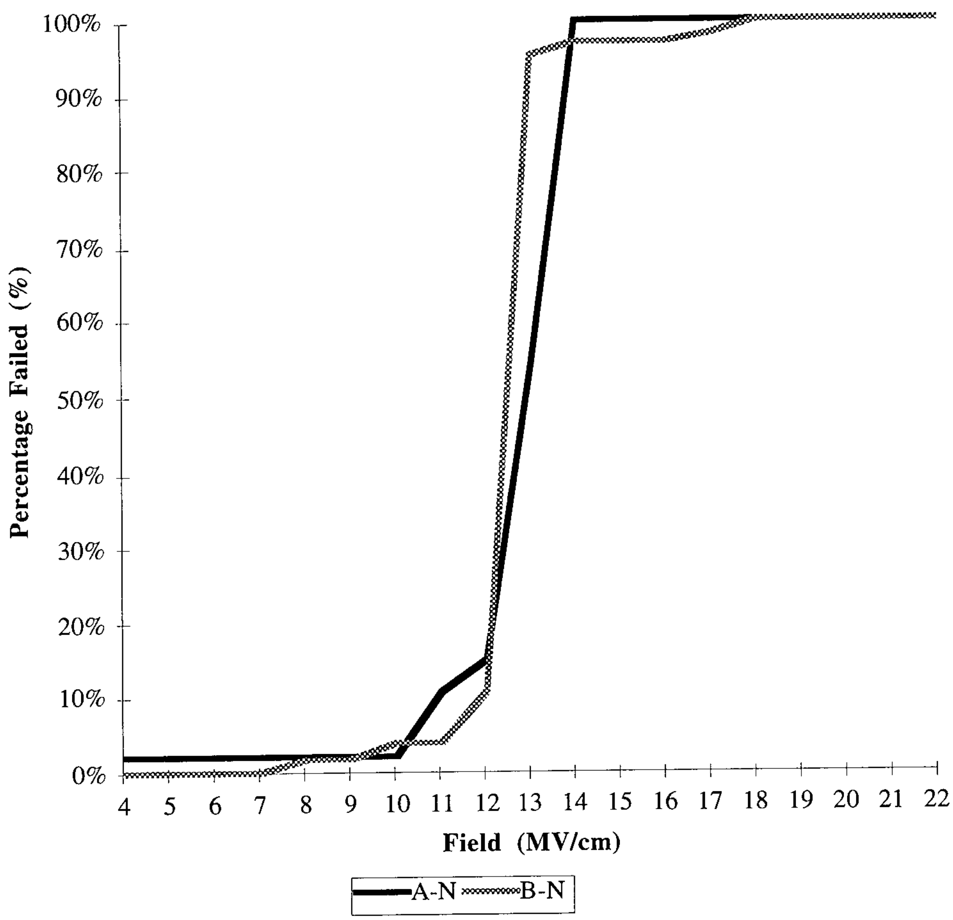

Figure 29. Uncensored Vendor A versus Vendor B cumulative breakdown curve for n capacitor data.

Figure 29 shows a comparison of the cumulative breakdown curves for the uncensored n capacitor populations of Vendor A and Vendor B. Of note is that Vendor A has its first oxide failure well before Vendor B, a higher percentage of the Vendor A failures is accounted for by values below the knee, and Vendor A reaches 100% failure at a higher field than Vendor B.

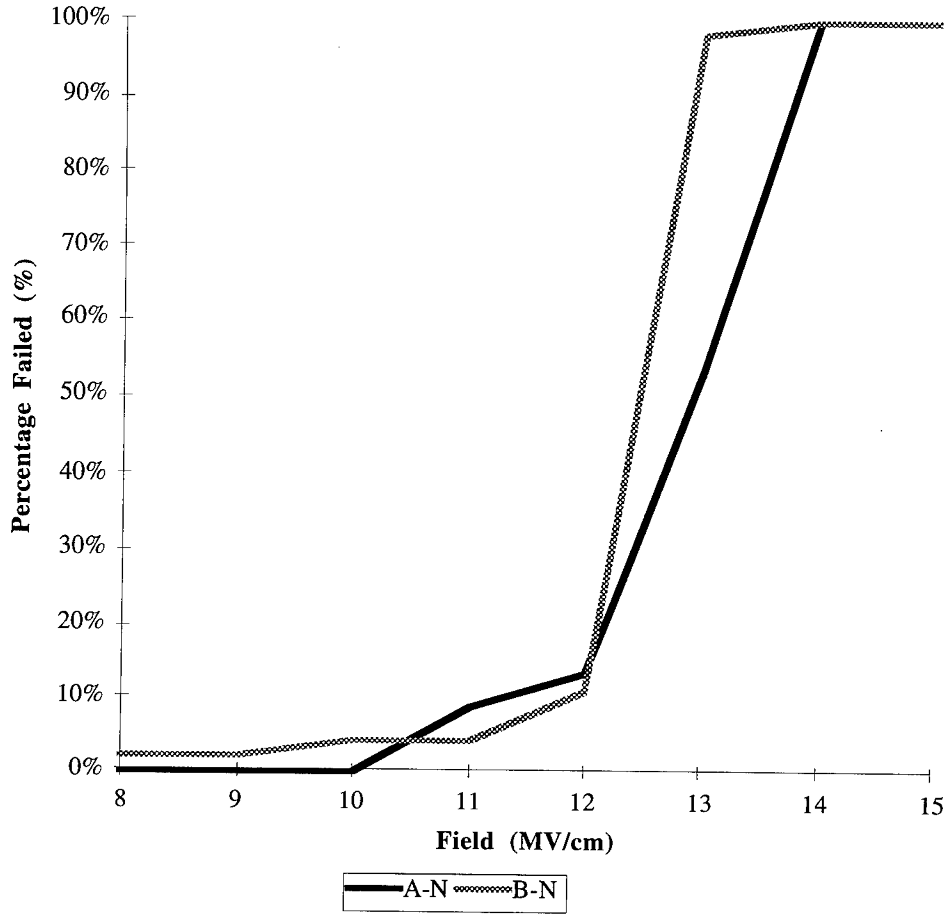

Figure 30. Censored Vendor A versus Vendor B cumulative breakdown curve for n capacitor data.

Figure 30 is a censored cumulative breakdown curve comparison of the Vendor A and Vendor B n capacitor populations. Now, Vendor A has its first failure at a field higher than Vendor B, Vendor A still high a higher percentage of failures accounted for below the knee of the curve, and Vendor A and Vendor B both reach 100% failure of the population at about the same time.

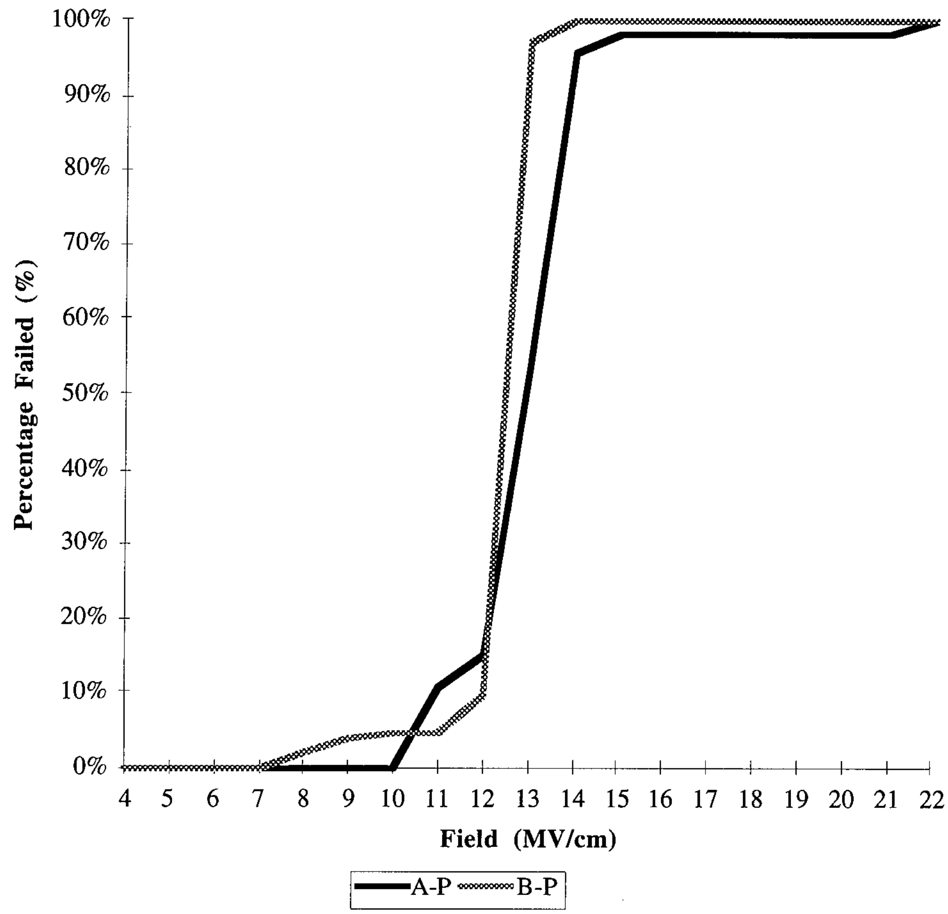

Figure 31. Uncensored Vendor A versus Vendor B cumulative breakdown curve for p capacitor data.

Figure 31 shows a comparison of the cumulative breakdown curves for the uncensored p capacitor populations of Vendor A and Vendor B. Of note is that Vendor B has its first oxide failure before Vendor A, a higher percentage of the Vendor A failures may be accounted for by values below the knee of the curve, and Vendor A reaches 100% failure at a higher field than Vendor B.

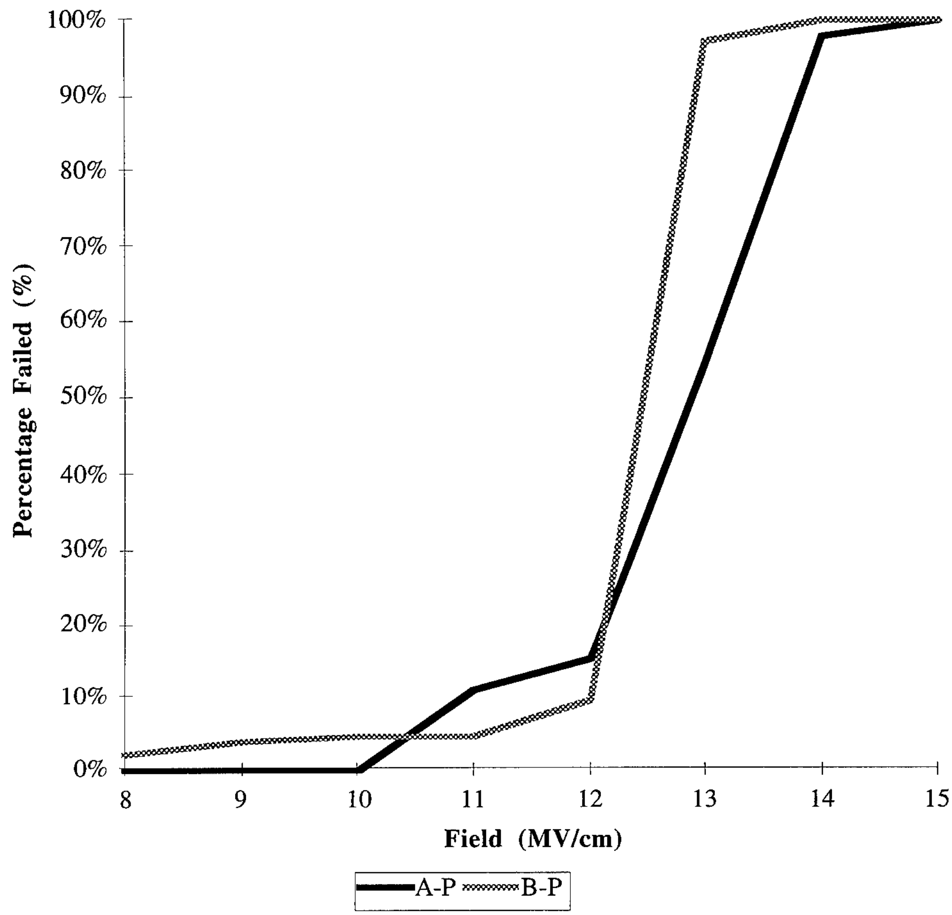

Figure 32. Censored Vendor A versus Vendor B cumulative breakdown curve for p capacitor data.

Figure 32 is a censored cumulative breakdown curve comparison of the Vendor A and Vendor B p capacitor populations. Vendor B still has its first failure at a field lower than Vendor A, Vendor A still has a higher percentage of failures accounted for below the knee of the curve, and Vendor A and Vendor B both reach 100% failure of the population at about the same time.

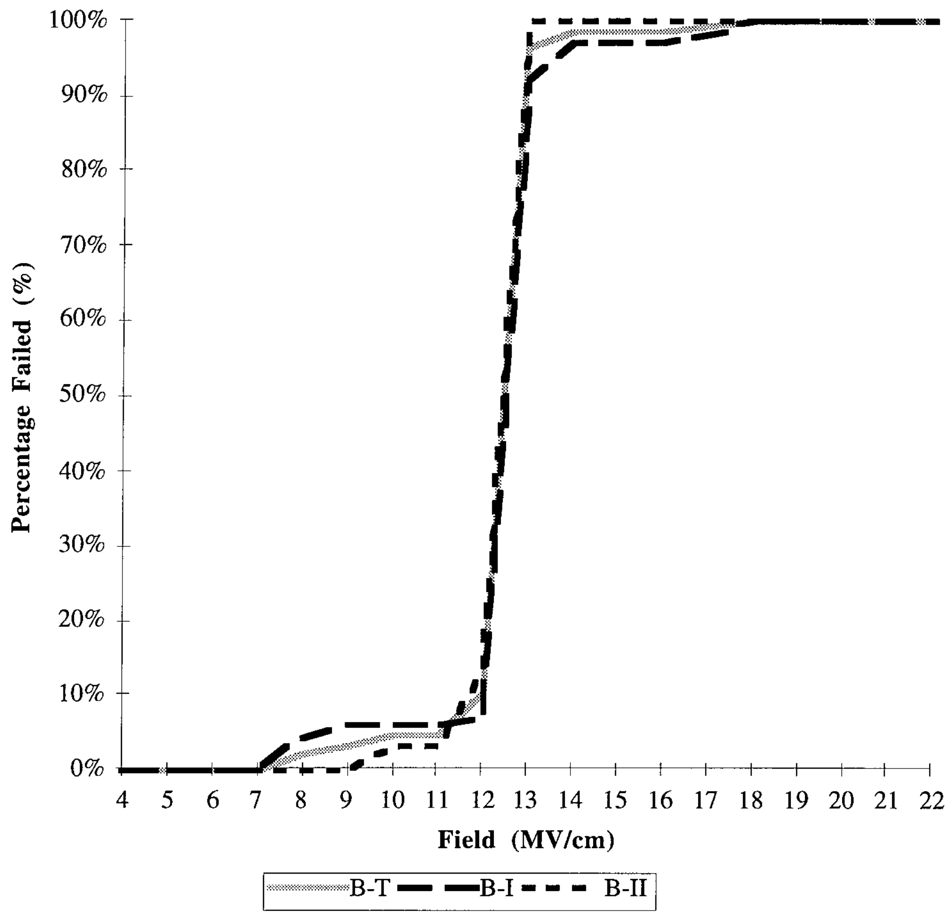

Figure 33. Uncensored Vendor B cumulative breakdown curve for wafer 1, wafer 2 and all capacitor data.

Figure 33 shows the uncensored cumulative breakdown curves for Vendor B capacitor population according to the wafer on which the tested capacitor was located.

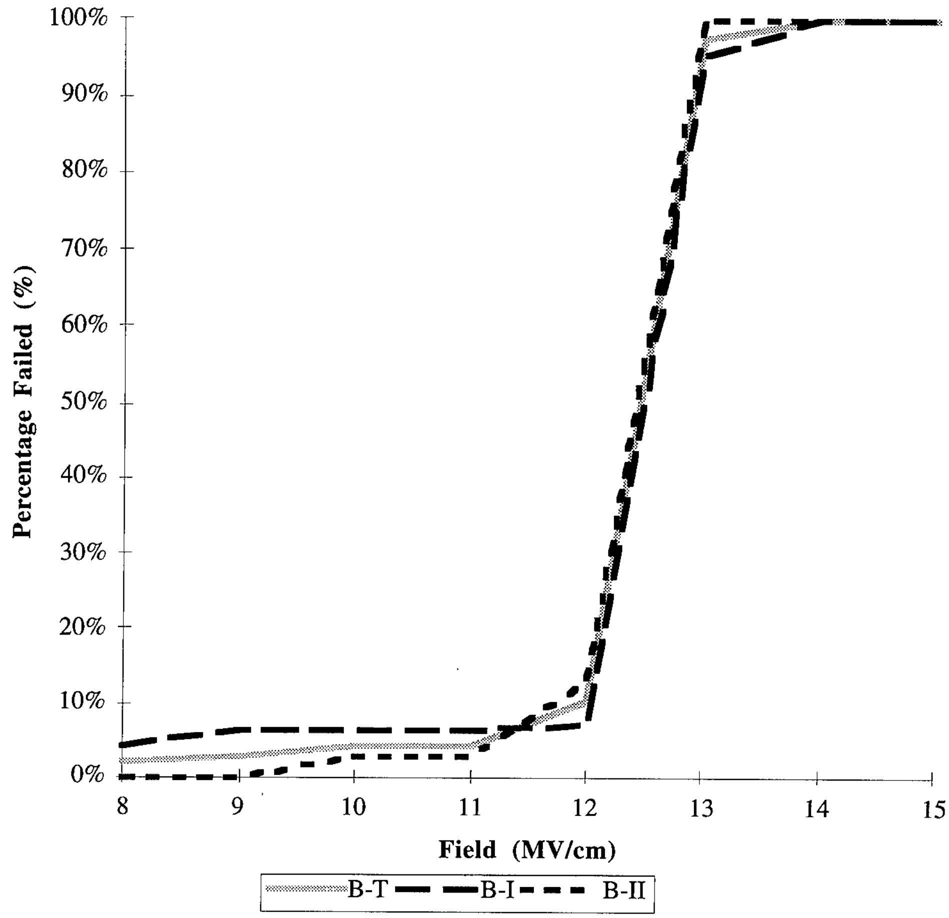

Figure 34. Censored Vendor B cumulative breakdown curve for wafer 1, wafer 2 and all capacitor data.

Figure 34 shows the censored cumulative breakdown curves for the Vendor B capacitor population according to the wafer on which the tested capacitor was located.

FUTURE

The continued assurance of reliable integrated circuits depends upon the quality of the oxides contained within the circuit. To assure that quality oxides are produced, there is still much work which needs to be performed in this area. From the physics of failure models which describe the phenomena to the test procedures used to monitor and detect oxide breakdown, many questions, concerns and arguments continue to be voiced.

Many new areas continue to crop up. In this vain, not only are gate oxides a concern, but interlevel dielectrics are beginning to be seen as problem areas. Interlevel dielectrics are beginning to see fields which produce stresses able to impact their reliability. In that regard, work on test structures and test procedures for interlevel dielectrics are needed. This is a relatively new area of concern which will become more important as the number of metal layers continue to increase.

Another important area which needs investigation is the affect of degradation of the oxide and its impact on oxide breakdown. As the intrinsic life of oxides is shortened by the increased fields experienced in normal use, a severe impact on oxide reliability will exist if this decreasing lifetime is further shortened by a degradation effect due to the electric fields experienced. This is a new question just beginning to be posed. As such, whether this is a real problem is not known.

Finally, with test times and the available silicon area decreasing, it is becoming increasingly important to develop novel structure designs and test methodologies. One such idea is the use of an arrayed oxide structure design to increase the testable area without increasing the number of probes. To take this idea one step further, the use of optical probes to reduce the probe pad size has even been discussed. Such a structure would be able to utilize more silicon, as the required probe space would be smaller than that for conventional mechanical probes. Also, test times would be reduced as the time to scratch the mechanical probe in would be eliminated. Finally, the speed with which such a test could be performed would be enhanced, as the optical generation of currents would help reduce the overall test time.

CONCLUSIONS

The voltage and current ramp test procedures are well defined within the JEDEC 14.2 standard and are easy to implement. By manufacturers using the standard, the end user is provided with the ability to compare test results at lab A with test results performed at lab B. The standard also allows the end user, himself, the ability to compare oxide quality between competing manufacturers. There is a problem, however, as the JEDEC procedure was arrived at in committee. The political process of the committee is compromise, sometimes to the detriment of the standard.

This particular standard is itself general in places, so that those participating had to change little with the way they were currently performing their tests. This standard's guidelines have several compromises relating to equipment capability, so that all participating in the committee could claim compliance with the standard procedure. No one wanted to have to go out and buy new equipment to be compliant with the standard. This political nature is one of the problems with industry committees. Although the compromises do not affect the technical merit of the procedure, they add just enough flexibility so that doubt may be cast on the direct comparison of two different manufacturers' test results.

ACKNOWLEDGMENTS

The author would like to thank Wilmar Sifre without whose help the testing would not have been accomplished; Daniel Burns, whose insightful knowledge of oxide breakdown stimulated the work; and Robert Hillman, without whose prodding the documentation of the work would not have been accomplished. Thanks is also due to Vance Tyree, University of Southern California Information Sciences Institute; Tim Turner, Turner Engineering Technology; and Mike Mitchell, Honeywell Inc., for help and insight throughout this work.

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1. J. Lee, I. C. Chen, and C. Hu, "Modeling and Characterization of Gate Oxide Reliability," IEEE Transactions on Electron Devices, vol 35, no. 12, p.2268, Dec 1988.

2. Joint Electronic Devices Engineering Council: Procedure for Wafer-Level Test of Thin Dielectrics. JESD-35, 1991.

APPENDIX A: HP4062B SYSTEM SPECIFICATION

Capacitance Measurement Subsystem

Hewlett Packard 4280A 1 MHz Capacitance Meter

Test Signal:

Frequency:	1MHz ± 0.01%
Level:	30mVrms ±10% or 10mVrms ±10%

Internal DC Bias:

Output:	0V to ± 100V
Ranges:	1V, 10V, and 100V
Ranging Modes:	Auto and Fixed

External Bias:

Maximum Voltage:	± 42V
Maximum Current:	± 100mA via EXT BIAS SLOW or EXT BIAS FAST

Table 16. Measurement Range Maximum Display and Maximum Digits.

Measurement Speed	Signal Level	Measurement Range		
		10pF/100µS	100pF/1mS	1nF/10mS
fast	10mV	19.00pF	190.0pF	1.900nF
	30mV			
med	10mV	120.0µS	1.200mS	12.00mS
	30mV	19.000pF	190.00pF	1.9000nF
slow	10mV			
	30mV	120.00µS	1.2000mS	12.000mS

Table 17. Auto Ranging Mode (V LIMIT = 0).

Voltage Range	Range Coverage	Resolution	Accuracy*
1V	±(0.000 to 1.999)V	1mV	± (0.2% + 0.01V)
10V	±(2.00 to 19.99)V	10mV	± (0.1% + 0.02V)
100V	± (20.0 to 100.0)V	100mV	± (0.1% + 0.1 V)

* Accuracy is calculated as ± (% of setting + offset).

Table 18. Fixed Ranging Mode (V LIMIT ≠ 0).

V LIMIT	Voltage Range	Range Coverage
0.001 to 1.999V	1V	± (0.000 to V LIMIT)V
2.00 to 19.99 V	10V	± (0.00 to V LIMIT)V
20.0 to 100.0 V	100V	± (0.0 to V LIMIT)V

* Accuracy and Resolution for each range are the same as those in Auto Ranging Mode.

DC Measurement Subsystem

Hewlett Packard 4141B DC Source/Monitor

SMU 1 High Sensitivity Source/Monitor Unit:

Table 19. High Sensitivity Current Source/Voltage Monitor Specification.

Voltage Full Scale Range	Sensitivity	Accuracy ±(% of rdg + % of range + volt)	Maximum Current
± 20V	1mV	±(0.1% + 0.05% + 0.5 • Io)	100mA
± 40V	2mV		50mA
±100V	5mV		20mA

Io=output current

Table 20. High Sensitivity Voltage Source/Current Monitor Specification.

Current Full Scale Range	Sensitivity	Accuracy ±(% of rdg + % of range + Amp)	Maximum Voltage
± 100mA	100μA	±[0.3% + (0.1 + 0.002 • Vo)%]	20V (>50mA) 40V (>20mA)
± 10mA	10μA		100V
±1000μA	1μA		
± 100μA	100nA		
± 10μA	10nA		
±1000nA	1nA		
± 100nA	100pA	±[0.5% + (0.1 + 0.002 • Vo)%]	
± 10nA	10pA	±[1% + (0.002 • Vo)% +15pA]	
±1000pA	1pA	±[1% + (0.002 • Vo)% + 8pA]	

Vo=output voltage

Input/Output Resistance:

Voltage Source/Current Monitor Mode: $< 0.5\Omega$

Current Source/Voltage Monitor Mode: $\geq 10^{12}\Omega$

Maximum Capacitance Load:

1000pF

Output Terminals:

High and Guard

DC Measurement Subsystem

Hewlett Packard 4141B DC Source/Monitor

SMU 2,3,4 Standard Source/Monitor Units

Table 21. Standard Current Source/Voltage Monitor Specification.

Voltage Full Scale Range	Sensitivity	Accuracy ±(% of rdg + % of range)	Maximum Current
± 20V	1mV	±(0.1% + 0.05%)	100mA
± 40V	2mV		50mA
±100V	5mV		20mA

Table 22. Standard Voltage Source/Current Monitor Specification.

Current Full Scale Range	Sensitivity	Accuracy ±(% of rdg + % of range + Amp)	Maximum Voltage
± 100mA	100µA	±[0.3% + (0.1+ 0.002 • Vo)%]	20V (>50mA) 40V (>20mA)
± 10mA	10µA		100V
±1000µA	1µA		
± 100µA	100nA		
± 10µA	10nA	±[0.3% + (0.003 • Vo)% + 10nA]	
±1000nA	1nA	±[0.5% + (0.001 • Vo)% + 2nA]	
± 100nA	100pA	±[0.5% + (0.1 • Vo)% + 1nA]	
± 10nA	10pA	Not Specified	
±1000pA	1pA		

Vo=output voltage

Input/Output Resistance:

Voltage Source/Current Monitor Mode: $\leq 10m\Omega$

Current Source/Voltage Monitor Mode: $\geq 10^{10}\Omega$

Maximum Capacitive Load:

1000pF

Output terminals:

High, Sense and Guard

DC Measurement Subsystem

Hewlett Packard 4141B DC Source/Monitor

Ground Unit:

Current Range:

± 500mA

Offset Voltage:

± 2mV max.

Voltage Source Units:

Table 23. VS Output Range, Resolution, and Accuracy.

Output Full Scale Range	Voltage Resolution	Accuracy	Maximum Current
±20V	±0.001V	± (0.5% setting ± 10mV)	10mA

Output Resistance:

≤ 1.5Ω

Maximum Capacitive Load:

200pF

Output terminals:

High and Guard

Voltage Monitor Units:

Table 24. VM Input Range, Sensitivity, and Accuracy.

Input Full Scale Range	Voltage Sensitivity	Accuracy
± 2V	± 0.0001V	±(0.5% rdg + 10mV)
±20V	± 0.001 V	±(0.2% rdg + 10mV)

Input Resistance:

1MΩ ± 1% in parallel with 1100pF

Input terminals:

High and Guard

Switching Matrix Subsystem

Hewlett Packard 4084B Switching Matrix Controller

Hewlett Packard 4085A Switching Matrix

Measurement pins:

48

Instrument Ports:

1 High Resolution SMU

3 Standard SMUs

1 Ground SMU

1 CMH

1 CML

2 AUX

Maximum Voltage between Instrument Ports:

±220V dc

Maximum Current at each Measurement Pin:

±500mA dc

Maximum Voltage at each Measurement Pin:

±100V dc

Maximum Stray Capacitance between Measurement Pins:

6pF

APPENDIX B: TEST PROGRAM

```
10   !*************************************************************************
20   !*****                                                               *****
30   !*****  J14_RAMPS                                                    *****
40   !*****                                                               *****
50   !*****  THIS PROGRAM PERFORMS THE JEDEC 14.2 OXIDE TESTS             *****
60   !*****  MUST BE LINKED WITH THE FOLLOWING:                           *****
70   !*****                                                               *****
80   !*****                 TIS, PARA                                     *****
90   !*****                                                               *****
100  !*************************************************************************
110  !*****                                                               *****
120  !*****  WRITTEN BY:    STEVEN L. DRAGER                              *****
130  !*****                                                               *****
140  !*****                                                               *****
150  !*****  REVISED BY:    STEVEN L. DRAGER                              *****
160  !*****                 WILMAR W. SIFRE                               *****
170  !*****                                                               *****
180  !*****                                                               *****
190  !*************************************************************************
200  !*****                                                               *****
210  !*****  DATA STORAGE IN BDAT FORMAT                                  *****
220  !*****  INFORMATION NEEDED WHEN CREATING A DATA FILE                 *****
230  !*****          REAL      ------> 8 bytes                            *****
240  !*****          INTEGER   ------> 2 bytes                            *****
250  !*****          STRING    ------> 1 byte/character + 1 pad byte      *****
260  !*****          if the string length is an odd number + a 4          *****
270  !*****          byte length header.                                  *****
280  !*****                                                               *****
290  !*************************************************************************
300  !*****                                                               *****
310  !*****  VARIABLE DECLARATIONS                                        *****
320  !*****                                                               *****
330  !*************************************************************************
340  !
350  DIM Capmeas(25)
360  DIM Capvoltage(25)
370  DIM Imeas(201),Ixptd(201),Volt(201)
380  REAL Efn,Bfn,Afn
390  REAL Caparea,Toxcalc,Cmax,Eox
400  REAL Capacitance,Fieldfac,Icheckpre,Icheckpos
410  !
420  !*************************************************************************
430  !*****                                                               *****
440  !*****  TECHNOLOGY VARIABLES                                         *****
450  !*****                                                               *****
460  !*************************************************************************
470  !*****                                                               *****
480  !*****                                                               *****
490  !*****                                                               *****
500  !*************************************************************************
510  !
520  Caparea=1.5876E-4                  !126um x 126um cm^2
530  !                                  tox=2.50E-6(250 Angstroms)
540  !                                  capacitance=2.2E-11 (22 picoFarads)
```

```
550   afnn=1.596E+8                          !FOWLER-NORDHEIM FUNCTION A
560   bfnn=350.97                            !FOWLER-NORDHEIM FUNCTION B
561   afnp=1.822E+7
562   bfnp=297.31
570   !
720   !**********************************************************************
730   !*****                                                            *****
740   !*****  VARIABLE INITIALIZATIONS                                  *****
750   !*****                                                            *****
760   !**********************************************************************
770   !
790   Eox=3.4531302E-13      ! Eox=Eo*Er where Er=3.9 and Eo=8.85418e-14 F/cm
800   !
810   !**********************************************************************
820   !*****                                                            *****
830   !*****  STRING INTIALIZATIONS                                     *****
840   !*****                                                            *****
850   !**********************************************************************
860   !
870   Clear_screen$=CHR$(255)&CHR$(75)                 !CLEAR CRT STRING
880   DUMP DEVICE IS 701                               !SET PLOT DEVICE
890   Page$=CHR$(12)                                   !PAGE PRINTER STRING
900   !
910   !**********************************************************************
920   !*****                                                            *****
930   !*****  INITIALIZE 4062A SEMICONDUCTOR PARAMETRIC TEST SYSTEM     *****
940   !*****                                                            *****
950   !**********************************************************************
960   !
970   Init_io
980   !
990   !**********************************************************************
1000  !*****                                                            *****
1010  !*****  INITIALIZE CAPACITANCE METER FOR CABLE LENGTH             *****
1020  !*****                                                            *****
1030  !**********************************************************************
1040  !
1050  OUTPUT 2;Clear_screen$;
1060  CLEAR 2724
1070  Connect(FNCmh,1)            !CONNECTS HIGH CAPACITANCE LEAD TO PIN 1
1080  Connect(FNCml,48)           !CONNECTS LOW CAPACITANCE LEAD TO PIN 48
1090  OUTPUT 2724;"CN10"          !CAPACITANCE CONNECTION MODE 10
1100  GOSUB Int_correct           !CAPACITANCE ZEROING SUBROUTINE
1110  GOSUB Reset                 !PIN GROUNDING SUBROUTINE
1120  !
1130  !**********************************************************************
1140  !*****                                                            *****
1150  !*****  PROGRAM MENU                                              *****
1160  !*****                                                            *****
1170  !**********************************************************************
1180  !
1190  PRINTER IS 1
1200  PRINT "1.  MEASURE FOWLER NORDHEIM"
1210  PRINT ""
```

```
1220 PRINT "2.  VOLTAGE RAMP STRESS"
1230 PRINT ""
1240 PRINT "3.  CURRENT RAMP STRESS"
1250 PRINT ""
1260 PRINT "4.  EXIT"
1270 PRINT ""
1280 INPUT "ENTER THE NUMBER OF THE ROUTINE YOU WISH TO PERFORM",Test_routine
1290 SELECT Test_routine
1300 !
1310 !**********************************************************************
1320 !*****                                                            *****
1330 !*****  MEASURE FOWLER NORDHEIM                                   *****
1340 !*****                                                            *****
1350 !**********************************************************************
1360 !
1370 CASE =1
1380   Cnt=201                            !5 to 25 MV/cm FIELD
1390   Fieldfac=.1                        !STEP .1 MV/cm
1400   Init_field=5                       !START FIELD
1410   Xvrpass=10                         !XAXIS VRAMP PLOT START VOLTAGE
1420   OUTPUT 2;Clear_screen$;
1430   GOSUB Define_file
1440   PRINTER IS 701
1450   File$=Wafer_id$&Type$&Chip_id$&"FN"
1460   CREATE ASCII File$,100
1470   ASSIGN @Path1 TO File$
1480   PRINT File$
1490   PRINT DATE$(TIMEDATE),TIME$(TIMEDATE)
1500   GOSUB Check
1510   Icheckpre=Icheck
1520   PRINT
1530   PRINT "PRE-STRESS CURRENT  ";Icheckpre
1540   PRINT
1550   IF ABS(Icheckpre)>1.0E-6 THEN GOTO 1650
1560   GOSUB Measure_cap
1570   GOSUB Measure_fn
1580   GOSUB Check
1590   GOSUB Plot_fn
1600   OUTPUT 701;Page$
1610   GOSUB Plot_vr
1620   Icheckpos=Icheck
1630   PRINT
1640   PRINT "POST-STRESS CURRENT  ";Icheckpos
1650   PRINTER IS 1
1660   ASSIGN @Path1 TO *
1670   OUTPUT 701;Page$
1680   GOTO 1190
1690 !
1700 !**********************************************************************
1710 !*****                                                            *****
1720 !*****  VRAMP STRESS                                              *****
1730 !*****                                                            *****
1740 !**********************************************************************
1750 !
```

```
1760  CASE =2
1770    Cnt=201                                  !1 to 20 MV/cm FIELD
1780    Xvrpass=0                                !XAXIS VRAMP PLOT START VOLTAGE
1790    Init_field=1                             !START FIELD
1800    OUTPUT 2;Clear_screen$;
1810    GOSUB Define_file
1820    IF Type$="N" THEN
1830      Afn=  afnn
1840      Bfn=  bfnn
1850    ELSE
1860      Afn=  afnp
1870      Bfn=  bfnp
1880    END IF
1890    PRINTER IS 701
1900    File$=Wafer_id$&Type$&Chip_id$&"VT"
1910    CREATE ASCII File$,100
1920    ASSIGN @Path1 TO File$
1930    PRINT File$
1940    PRINT DATE$(TIMEDATE),TIME$(TIMEDATE)
1950    GOSUB Check
1960    Icheckpre=Icheck
1970    PRINT "PRE-STRESS CURRENT = ";Icheckpre
1980    IF ABS(Icheckpre)>1.0E-6 THEN GOTO 2070
1990    GOSUB Measure_cap
2000    GOSUB Voltage_stress
2010    GOSUB Check
2020    GOSUB Plot_vr
2030    GOSUB Plot_fn
2040    GOSUB Plot_vr
2050    Icheckpos=Icheck
2060    PRINT "POST-STRESS CURRENT = ";Icheckpos
2070    PRINTER IS 1
2080    ASSIGN @Path1 TO *
2090    OUTPUT 701;Page$
2100    GOTO 1190
2110  !
2410  !************************************************************************
2420  !*****                                                             *****
2430  !*****   END PROGRAM EXECUTION                                     *****
2440  !*****                                                             *****
2450  !************************************************************************
2460  !
2470  CASE =4
2480    OUTPUT 2;Clear_screen$;
2490    GOTO End
2500  !
2510  !************************************************************************
2520  !*****                                                             *****
2530  !*****   INVALID INPUT FOR MENU RESPONSE                           *****
2540  !*****                                                             *****
2550  !************************************************************************
2560  !
2570  CASE ELSE
2580    BEEP
```

```
2590     PRINT "INVALID INPUT"
2600     INPUT "ENTER THE NUMBER OF THE ROUTINE YOU WISH TO PERFORM",Test_routine
2610     GOTO 1290
2620  END SELECT
2630  !
2640  !**************************************************************************
2650  !*****                                                                *****
2660  !*****  SUBROUTINES                                                   *****
2670  !*****                                                                *****
2680  !**************************************************************************
2690  !
2700 Int_correct:  !
2710   !
2720  Srq=2
2730  Data_ready=0
2740  Status_byte=0
2750  ON INTR 27 GOSUB Cal_end
2760  DISP "DISCONNECT DUT"
2770  PAUSE
2780  OUTPUT 2724;"LE3"                              !CABLE LENGTH 0-5 meters
2790  OUTPUT 2724;"MD1"                              !DATA READY SRQ MASK OFF
2800  ENABLE INTR 27;Srq
2810  OUTPUT 2724;"CA"                               !START CALIBRATION
2820   !
2830 Cable_open:  !
2840   !
2850  IF BIT(Status_byte,Data_ready)=1 THEN GOTO Zero_open
2860  GOTO Cable_open
2870   !
2880 Zero_open:  !
2890   !
2900  Status_byte=0
2910  DISP "CONNECT GROUND"
2920  PAUSE
2930  OUTPUT 2724;"ZO"                               !ZERO OPEN
2940   !
2950 Idle_open:  !
2960   !
2970  IF BIT(Status_byte,Data_ready)=1 THEN GOTO Zero_open_end
2980  GOTO Idle_open
2990   !
3000 Zero_open_end:  !
3010   !
3020  OUTPUT 2724;"MD0"                              !DATA READY SRQ MASK ON
3030  OUTPUT 2724;"CE1"                              !CORRECTION ENABLE ON
3040  DISP "CONNECT DUT"
3050  PAUSE
3060  RETURN
3070   !
3080 Cal_end:  !
3090   !
3100  Status_byte=SPOLL(2724)
3110  ENABLE INTR 27;Srq
3120  RETURN
```

```
3130   !
3140 Reset:  !
3150   !
3160  Force_v(FNSmu(1),0)
3170  Connect(FNGnd,1,48)
3180  RETURN
3190   !
3200 Check:  !
3210   !
3220  Connect(FNSmu(1),1)
3230  Force_v(FNSmu(1),5*Captype)
3240  Measure_i(FNSmu(1),Icheck)
3250  GOSUB Reset
3260  OUTPUT @Path1;Icheck
3270  RETURN
3280   !
3290 Define_file:   !
3300   !
3310  INPUT "WAFER INDENTIFICATION NUMBER (ALPHA-NUMERICS)",Wafer_id$[1,5]
3320  INPUT "CHIP NUMBER",Chip_id$
3330  INPUT "CAPACITOR TYPE (P/N)",Type$
3340  IF Type$="N" THEN GOTO 3370
3350  IF Type$="P" THEN GOTO 3390
3360  GOTO 3330
3370  Captype=-1
3380  GOTO 3400
3390  Captype=1
3400  RETURN
3410   !
3420 Measure_fn:   !
3430   !
3440   !***********************************************************************
3450   !*****                                                             *****
3460   !***** J=AE^2EXP(-B/E)                                             *****
3470   !***** J-current density=current/area                              *****
3480   !***** A-constant to be found                                      *****
3490   !***** E-field=voltage/oxide thickness                             *****
3500   !***** B-constant to be found                                      *****
3510   !*****                                                             *****
3520   !***********************************************************************
3530   !
3540  Ymin=1.E-1
3550  Ymax=1.E-12
3560  Connect(FNSmu(1),1)
3570  Connect(FNGnd,48)
3580  FOR I=0 TO Cnt
3581     Field_val=I*Fieldfac+Init_field
3582     Volt(I)=Field_val*Toxcalc*1.E+6
3600     IF Volt(I)>=100 THEN GOTO 3730
3610     Force_v(FNSmu(1),Volt(I)*Captype,100,2.0E-2)
3620     Measure_i(FNSmu(1),Imeas(I))
3630     IF Imeas(I)=0 THEN GOTO 3730
3631     IF I=0 THEN GOTO 3640
3636     IF ABS(Imeas(I))>=.019 AND ABS(Imeas(I-1))<.019 THEN Vbd=Volt(I-1)
```

```
3640      IF ABS(Imeas(I))<Ymin THEN
3650        Ymin=ABS(Imeas(I))
3660        Fieldmin=Init_field+(I*Fieldfac)
3670      END IF
3680      IF ABS(Imeas(I))>Ymax THEN
3690        Ymax=ABS(Imeas(I))
3700        Fieldmax=Init_field+(I*Fieldfac)
3710      END IF
3720    NEXT I
3730    GOSUB Reset
3740    OUTPUT @Path1;Imeas(*)
3750    RETURN
3760      !
3770 Plot_fn:   !
3780      !
3790      !*********************************************************************
3800      !*****                                                           *****
3810      !*****  J=AE^2EXP(-B/E)                                          *****
3820      !*****  LOG(J/E^2)=LOG(A)-B/E                                    *****
3830      !*****  y=LOG(J/E^2)                                             *****
3840      !*****  m=-B                                                     *****
3850      !*****  x=1/E                                                    *****
3860      !*****  b=LOG(A)                                                 *****
3870      !*****  m=Y1-Y2/X1-X2   B=-m                                     *****
3880      !*****  b=y-mx=LOG(J/E^2)+B*(1/E)    A=EXP(b)                    *****
3890      !*****                                                           *****
3900      !*********************************************************************
3910      !
3920    Xmax=.2
3930    Yminfn=LOG((Ymin/Caparea)/(Fieldmin*Fieldmin))-1
3940    Ymaxfn=LOG((Ymax/Caparea)/(Fieldmax*Fieldmax))
3950                                Loggraph(Xmax,10^Yminfn,10^Ymaxfn,.04,Toxcalc,"1/FIELD
(cm/MV)","LOG(J/FIELD^2)","FOWLER-NORDHEIM CURRENT",1,1)
3960    FOR I=0 TO Cnt
3970      IF Imeas(I)=0 THEN GOTO 4030
3980      Field=Init_field+(I*Fieldfac)
3990      J=ABS(Imeas(I))/Caparea                         ! CURRENT DENSITY (A/cm^2)
4000      IF I=0 THEN MOVE (1/Field),LOG(J/(Field*Field))
4010      DRAW (1/Field),LOG(J/(Field*Field))
4020    NEXT I
4030    INPUT "ENTER VALUE FOR X1,X2",X1,X2
4040    I1=PROUND((((1/X1)-Init_field)/Fieldfac),0)
4050    I2=PROUND((((1/X2)-Init_field)/Fieldfac),0)
4060    Y1=LOG((ABS(Imeas(I1)/Caparea))/((I1*Fieldfac+Init_field)^2))     ! A/(MV)^2
4070    Y2=LOG((ABS(Imeas(I2)/Caparea))/((I2*Fieldfac+Init_field)^2))     ! A/(MV)^2
4080    Bfn=-1*((Y1-Y2)/(X1-X2))                                          ! Bfn   (A/MV*cm)
4090    Afn=EXP(Y1+(Bfn*X1))                                              ! Afn   (A/(MV^2))
4100    PRINT "X1 =";X1,"                     X2 =";X2
4110    PRINT "A_FN=";Afn,"B_FN=";Bfn
4120    PRINT
4130    PRINT
4140    ON ERROR GOTO 4240
4150    FOR I=0 TO Cnt
4160      Field_val=(I*Fieldfac+Init_field)
```

```
4170      Ixptd(I)=Caparea*Afn*Field_val*Field_val*EXP(-Bfn/Field_val)
4180      J=ABS(Ixptd(I))/Caparea
4190      IF I=0 THEN MOVE 1/Field_val,LOG(J/(Field_val*Field_val))
4200      DRAW 1/Field_val,LOG(J/(Field_val*Field_val))
4210   NEXT I
4220   DUMP GRAPHICS
4230   GRAPHICS OFF
4240   RETURN
4250   !
4260 Plot_vr:    !
4270   !
4280   Yminvr=LGT(Ymin)-1
4290   Ymaxvr=LGT(Ymax)
4300            Loggraph(60,10^Yminvr,10^Ymaxvr,Xvrpass,Toxcalc,"VOLTAGE","LOG-CURRENT","VRAMP STRESS",0,1)
4310   FOR I=0 TO Cnt
4320     IF Imeas(I)=0 THEN GOTO 4380
4330     Field_val=(I*Fieldfac+Init_field)
4340     Voltage=Field_val*Toxcalc*1.E+6
4350     IF I=0 THEN MOVE Voltage,LGT(ABS(Imeas(0)))
4360     DRAW Voltage,LGT(ABS(Imeas(I)))
4370   NEXT I
4380   FOR Ix=1 TO 3
4390     FOR I=0 TO Cnt
4400       Field_val=(I*Fieldfac+Init_field)
4410       Voltage=Field_val*Toxcalc*1.E+6
4420       IF Voltage>=40 THEN GOTO 4590
4430       Ixptd(I)=Caparea*Afn*Field_val*Field_val*EXP(-Bfn/Field_val)
4440       IF Ix=1 THEN
4450         IF I=0 THEN MOVE Voltage,LGT(ABS(Ixptd(0)))
4460         DRAW Voltage,LGT(ABS(Ixptd(I)))
4470       END IF
4480       IF Ix=2 THEN
4490         IF I=0 THEN MOVE Voltage,LGT(ABS(Ixptd(0)))
4500         LINE TYPE 5
4510         DRAW Voltage,LGT((ABS(Ixptd(I)))*10)
4520       END IF
4580     NEXT I
4590   NEXT Ix
4600   DUMP GRAPHICS
4610   GRAPHICS OFF
4620   RETURN
4630   !
4640 Measure_cap:   !
4650   !
4660   !**********************************************************************
4670   !*****                                                           *****
4680   !*****  Tox=Eox*Caparea/Capcalc                                  *****
4690   !*****  Tox-oxide thickness                                      *****
4700   !*****  Eox-permittivity=3.46E-13F/cm                            *****
4710   !*****  Caparea-area of capacitor                                *****
4720   !*****  Capcalc-capacitance                                      *****
4730   !*****                                                           *****
4740   !**********************************************************************
```

```
4750   !
4760   Cmax=0
4770   Cnt1=0
4780   Toxcalc=0
4790   Connect(FNCmh,1)
4800   Connect(FNCml,48)
4810   OUTPUT 2724;"FN2"                    !CAPACITANCE MEASUREMENT MODE
4820   OUTPUT 2724;"IB2"                    !SINGLE SIDED RAMP VOLTAGE
4830   OUTPUT 2724;"PS-6"                   !START VOLTAGE
4840   OUTPUT 2724;"PP6"                    !STOP VOLTAGE
4850   OUTPUT 2724;"PE.5"                   !STEP VOLTAGE
4860   OUTPUT 2724;"PL1"                    !HOLD TIME
4870   OUTPUT 2724;"PD1"                    !STEP DELAY
4880   OUTPUT 2724;"BC"                     !CLEAR DATA BUFFER
4890   OUTPUT 2724;"SW1"                    !START SWEEP
4900   ENTER 2724;Capmeas(Cnt1),Capvoltage(Cnt1)
4910   IF ABS(Capmeas(Cnt1))>Cmax THEN Cmax=ABS(Capmeas(Cnt1))
4920   IF Capvoltage(Cnt1)=6 THEN GOTO 4950
4930   Cnt1=Cnt1+1
4940   GOTO 4900
4950   OUTPUT 2724;"SW0"                    !STOP SWEEP
4960   OUTPUT 2724;"IB1"                    !DC VOLTAGE
4970   OUTPUT 2724;"PV0"                    !OUTPUT ZERO VOLTS
4980   Connect(FNGnd,1,48)
4990   Cvgraph(6,1,"BIAS","C/COX","C-V CHARACTERISTICS",1)
5000   FOR I=0 TO Cnt1
5010     IF I=0 THEN MOVE -6,ABS(Capmeas(0)/Cmax)
5020     DRAW Capvoltage(I),ABS(Capmeas(I))/Cmax
5030   NEXT I
5040   INPUT "WANT TO RE-DO THE C/V PLOT (Y/N)",Ans$
5050   IF Ans$="Y" THEN GOTO 4760
5060   OUTPUT @Path1;Capmeas(*)
5070   DUMP GRAPHICS
5080   GRAPHICS OFF
5090   IF Type$="N" THEN Capacitance=ABS(Capmeas(22))                    ! Farads
5100   IF Type$="P" THEN Capacitance=ABS(Capmeas(2))                     ! Farads
5110   Toxcalc=Eox*Caparea/Capacitance                                   ! cm
5120   PRINT "CALCULATED TOX=";Toxcalc;"  MEASURED CAPACITANCE=";Capacitance
5130   PRINT
5140   RETURN
5150   !
5160 Voltage_stress:  !
5170   !
5180   !**********************************************************************
5190   !*****                                                           *****
5200   !*****  J=AE^2EXP(-B/E)                                          *****
5210   !*****  I=(AREA)AE^2EXP(-B/E)                                    *****
5220   !*****                                                           *****
5230   !**********************************************************************
5240   !
5250   Ymin=1.E-1
5260   Ymax=1.E-12
5270   Connect(FNSmu(1),1)
5280   Connect(FNGnd,48)
```

```
5290  INPUT "ENTER RATE FOR ELECTRIC FIELD (.1MV/cm*S - 1 MV/cm*S)",Fieldfac
5300  FOR I=0 TO Cnt
5310     Field_val=I*Fieldfac+Init_field
5320     Volt(I)=Field_val*Toxcalc*1.E+6                          ! Volts
5330     IF I=0 THEN
5340        PRINT "INITIAL VOLTAGE =";Volt(I)
5350        PRINT "E-FIELD RATE =";Fieldfac;" MV/cm*sec"
5360     END IF
5370     IF Volt(I)>=100 THEN GOTO 5530
5380     Ixptd(I)=Caparea*Afn*Field_val*Field_val*EXP(-Bfn/Field_val)
5390     Force_v(FNSmu(1),Captype*Volt(I),100,2.E-2)
5400     WAIT .9
5410     Measure_i(FNSmu(1),Imeas(I))
5420     IF ABS(Imeas(I))<Ymin THEN
5430        Ymin=ABS(Imeas(I))
5440        Fieldmin=(I*Fieldfac)+Init_field
5450     END IF
5460     IF ABS(Imeas(I))>Ymax THEN
5470        Ymax=ABS(Imeas(I))
5480        Fieldmax=(I*Fieldfac)+Init_field
5490     END IF
5500     IF I=0 THEN GOTO 5520
5510     IF ABS(Imeas(I))>=.049 AND ABS(Imeas(I-1))<.049 THEN Vbd=Volt(I-1)
5511     IF ABS(Imeas(I))>=.049 AND ABS(Imeas(I-1))>=.049 THEN GOTO 5530
5520  NEXT I
5530  PRINT "FINAL VOLTAGE =";Volt(I-1)
5540  OUTPUT @Path1;Fieldfac,Imeas(*)
5550  GOSUB Reset
5560  PRINT "BREAKDOWN VOLTAGE = ";Vbd
5570  RETURN
5580   !
5620   !
5630 End:  !
5640   !
5650  PRINT "PROGRAM TERMINATED"
5660  END
5670   !
5680   !*********************************************************************
5690   !*********************************************************************
5700   !*********************************************************************
5710  SUB Lingraph(Xmax,Ymax,Xname$,Yname$,Title$,OPTIONAL INTEGER Gridding)
5720    DEG
5730    GINIT
5740    GRAPHICS ON
5750    WINDOW 0,100,0,100
5760    MOVE 50,100
5770    LORG 6
5780    LABEL Title$
5790    MOVE 50,7.5
5800    CSIZE 3
5810    LORG 4
5820    LABEL Xname$
5830    LORG 6
5840    LDIR 90
```

```
5850    MOVE 0,50
5860    LABEL Yname$
5870     Getaxis(Xmax,Xmaxaxis,Xminortic,Xmajortic)
5880     Getaxis(Ymax,Ymaxaxis,Yminortic,Ymajortic)
5890     VIEWPORT RATIO*12,RATIO*95,17,95
5900     WINDOW 0,Xmaxaxis,0,Ymaxaxis
5910     AXES Xminortic,Yminortic,0,0,Xmajortic/Xminortic,Ymajortic/Yminortic
5920    CLIP OFF
5930    LORG 6
5940    LDIR 0
5950     FOR Xlabelpos=0 TO Xmaxaxis*(1+1.E-12) STEP SGN(Xmax)*Xmajortic
5960       MOVE Xlabelpos,0
5970       LABEL Xlabelpos
5980    NEXT Xlabelpos
5990    LORG 8
6000     FOR Ylabelpos=0 TO Ymaxaxis*(1+1.E-12) STEP SGN(Ymax)*Ymajortic
6010       MOVE 0,Ylabelpos
6020       LABEL USING "K";Ylabelpos
6030    NEXT Ylabelpos
6040    CLIP ON
6050    IF NPAR=6 THEN
6060      IF Gridding THEN
6070        LINE TYPE 4
6080         GRID Xmajortic,Ymajortic,0,0
6090        LINE TYPE 1
6100      END IF
6110    END IF
6120    MOVE 0,0
6130  SUBEND          !
6140  !************************************************************************
6150  SUB Cvgraph(Xmax,Ymax,Xname$,Yname$,Title$,OPTIONAL INTEGER Gridding)
6160    DEG
6170    GINIT
6180    GRAPHICS ON
6190    WINDOW 0,100,0,100
6200    MOVE 50,100
6210    LORG 6
6220    LABEL Title$
6230    MOVE 50,7.5
6240    CSIZE 3
6250    LORG 4
6260    LABEL Xname$
6270    LORG 6
6280    LDIR 90
6290    MOVE 0,50
6300    LABEL Yname$
6310     Getaxis(Xmax,Xmaxaxis,Xminortic,Xmajortic)
6320     Getaxis(Ymax,Ymaxaxis,Yminortic,Ymajortic)
6330     VIEWPORT RATIO*6,RATIO*99,14,92
6340     WINDOW -Xmaxaxis,Xmaxaxis,0,Ymaxaxis
6350     AXES Xminortic,Yminortic,-Xmaxaxis,0,Xmajortic/Xminortic,Ymajortic/Yminortic
6360    CLIP OFF
6370    LORG 6
6380    LDIR 0
```

```
6390     FOR Xlabelpos=-Xmaxaxis TO Xmaxaxis*(1+1.E-12) STEP SGN(Xmax)*Xmajortic
6400       MOVE Xlabelpos,0
6410       IF ABS(Xmaxaxis)>1.E+6*ABS(Xlabelpos) THEN Xlabelpos=0
6420       LABEL Xlabelpos
6430     NEXT Xlabelpos
6440     LORG 8
6450     FOR Ylabelpos=0 TO Ymaxaxis*(1+1.E-12) STEP SGN(Ymax)*Ymajortic
6460       MOVE -Xmaxaxis,Ylabelpos
6470       LABEL USING "K";Ylabelpos
6480     NEXT Ylabelpos
6490     CLIP ON
6500     IF NPAR=6 THEN
6510       IF Gridding THEN
6520         LINE TYPE 4
6530         GRID Xmajortic,Ymajortic,0,0
6540         LINE TYPE 1
6550       END IF
6560     END IF
6570     MOVE -Xmaxaxis,0
6580   SUBEND          !
6590   !************************************************************************
6600     SUB   Loggraph(Xmax,Ymin,Ymax,Zeropass,Toxcalc,Xname$,Yname$,Title$,Topaxis,OPTIONAL
INTEGER Gridding)
6610     INTEGER Yminaxis,Ymaxaxis,Yminortic,Ymajortic,I,Gridflag
6620     Gridflag=0
6630     IF NPAR=10 THEN
6640       IF Gridding THEN Gridflag=1
6650     END IF
6660     Xmax=DROUND(Xmax,12)
6670     Ymin=DROUND(Ymin,12)
6680     Ymax=DROUND(Ymax,12)
6690     DEG
6700     GINIT
6710     GRAPHICS ON
6720     WINDOW 0,100,0,100
6730     MOVE 50,100
6740     LORG 6
6750     LABEL Title$
6760     MOVE 50,7.5
6770     CSIZE 3
6780     LORG 4
6790     LABEL Xname$
6800     LORG 6
6810     LDIR 90
6820     MOVE 0,50
6830     LABEL Yname$
6840     Getaxis(Xmax,Xmaxaxis,Xminortic,Xmajortic)
6850     Getlogaxis(Ymin,Ymax,Yminaxis,Ymaxaxis,Yminortic,Ymajortic)
6860     VIEWPORT RATIO*6.5,RATIO*97,14,93
6870     WINDOW Zeropass,Xmax,Yminaxis,Ymaxaxis              ! XMAXAXIS   <-- XMAX
6880     AXES Xminortic,1,Zeropass,Yminaxis,Xmajortic/Xminortic
6890     CLIP OFF
6900     LORG 6
6910     LDIR 0
```

```
6920   !
6930   FOR Xlabelpos=Zeropass TO Xmaxaxis*(1+1.E-12) STEP SGN(Xmax)*Xmajortic
6940     MOVE Xlabelpos,Yminaxis-.1
6950     LABEL Xlabelpos
6960     IF Topaxis THEN
6970       MOVE Xlabelpos,Ymaxaxis+.72
6980       IF Xlabelpos=0 THEN GOTO 7040
6990       LABEL DROUND(((1/Xlabelpos)*Toxcalc*1.E+6),3)
7000     ELSE
7010       MOVE Xlabelpos,Ymaxaxis+.38
7020       IF Xlabelpos=0 THEN GOTO 7040
7030       LABEL DROUND(((Xlabelpos*1.E-6)/Toxcalc),3)
7040     END IF
7050   NEXT Xlabelpos
7060   LORG 8
7070   !
7080   IF Ymajortic THEN
7090     FOR Ylabelpos=Yminaxis TO Ymaxaxis*(1+SGN(Ymaxaxis)*1.E-12)
7100       MOVE Zeropass,Ylabelpos
7110       LABEL USING "MDD";SGN(Ymax)*Ylabelpos
7120     NEXT Ylabelpos
7130   ELSE
7140     FOR Ylabelpos=10^Yminaxis TO 10^Ymaxaxis*(1+1.E-12) STEP 10^Yminaxis
7150       MOVE Zeropass,LGT(Ylabelpos)                 ! .01*Xmaxaxis: tic length
7160       DRAW Zeropass,LGT(Ylabelpos)
7170       LABEL USING "MDE";SGN(Ymax)*Ylabelpos
7180     NEXT Ylabelpos
7190   END IF
7200   !
7210   CLIP ON
7220   IF Yminortic THEN                                ! minortic=majortic
7230     IF Gridflag THEN
7240       LINE TYPE 4
7250       GRID Xmajortic,1,Zeropass,Yminaxis
7260       LINE TYPE 1
7270     END IF
7280   ELSE
7290     IF Gridflag THEN
7300       LINE TYPE 4
7310       GRID Xmajortic,0,Zeropass,Yminaxis                     ! draw x grid
7320       LINE TYPE 1
7330     END IF
7340     I=2
7350     J=1
7360     LOOP
7370       Ygridpos=I*J*10^Yminaxis
7380     EXIT IF Ygridpos>(10^Ymaxaxis)*(1+1.E-12)
7390       MOVE Zeropass,LGT(Ygridpos)
7400       IDRAW .005*Xmaxaxis,0                        ! .005*Xmaxaxis: tic length
7410       IF Gridflag THEN
7420         LINE TYPE 4
7430         IDRAW Xmaxaxis,0
7440         LINE TYPE 1
7450       END IF
```

```
7460        I=I+1
7470        IF I=10 THEN
7480          I=1
7490          J=J*10
7500        END IF
7510      END LOOP
7520    END IF
7530    MOVE 0,Yminaxis
7540  SUBEND           !
7550  !***********************************************************************
7560  SUB Getaxis(Maxval,Maxaxis,Minortic,Majortic)
7570    OPTION BASE 1
7580    DIM Maxval$[10]
7590    INTEGER Manti
7600    OUTPUT Maxval$ USING "SDE";Maxval
7610    Manti=VAL(Maxval$[2,2])
7620    Exponent=10^VAL(Maxval$[4])
7630    IF ABS(DROUND(Manti*Exponent,12))<ABS(DROUND(Maxval,12)) THEN Manti = Manti + 1
7640    IF Manti=10 THEN
7650      Manti=1
7660      Exponent=Exponent*10
7670    END IF
7680    SELECT Manti
7690    CASE 1
7700      Minortic=.05
7710      Majortic=.1
7720    CASE 2,3
7730      Minortic=.1
7740      Majortic=.5
7750    CASE 4 TO 9
7760      Minortic=.5
7770      Majortic=1
7780    END SELECT
7790    Maxaxis=DROUND(SGN(Maxval)*Manti*Exponent,12)
7800    Minortic=DROUND(Minortic*Exponent,12)
7810    Majortic=DROUND(Majortic*Exponent,12)
7820  SUBEND           !
7830  !***********************************************************************
7840  SUB Getlogaxis(Minval,Maxval,INTEGER Minaxis,Maxaxis,Minortic,Majortic)
7850  !
7860  ! Majortic,Minortic:  return 0 if the tic interval is 1/10 decades,
7870  ! return 1 if the tic interval is a decade.
7880  !
7890    Maxval=DROUND(Maxval,12)
7900    Maxaxis=INT(LGT(ABS(Maxval)))
7910    IF Maxaxis<DROUND(LGT(ABS(Maxval)),12) THEN Maxaxis=Maxaxis+1
7920    Minval=DROUND(Minval,12)
7930    Minaxis=INT(LGT(ABS(Minval)))
7940    IF Minaxis>DROUND(LGT(ABS(Minval)),12) THEN Minaxis=Minaxis-1
7950    SELECT Maxaxis-Minaxis
7960    CASE 1
7970      Minortic=0
7980      Majortic=0
7990    CASE 2 TO 6
```

```
8000       Minortic=0
8010       Majortic=1
8020     CASE >6
8030       Minortic=1
8040       Majortic=1
8050     END SELECT
8060   SUBEND            !
8070   !**********************************************************************
```

APPENDIX C: DATA

Table 25. Vendor A Fowler-Nordheim Data.

chip #	Cox (F)	Tox (cm)	Ipre (A)	Bkv (V)	Mode	Rate (MV/cm)	Field (MV/cm)	Afn	Bfn
004n	1.914E-11	1.916E-06	2.345E-08	27.13	c	0.1	11.90	5.345E+14	411.32
005n	1.921E-11	1.909E-06	3.635E-09	22.44	c	0.1	11.76	2.570E+14	400.10
013n	1.894E-11	1.936E-06	1.679E-09	26.91	c	0.1	13.88	3.975E+15	405.30
014n	1.964E-11	1.867E-06	9.235E-08	26.89	c	0.1	14.40	2.582E+16	543.83
015n	1.963E-11	1.867E-06	2.692E-09	21.69	c	0.1	11.62	4.065E+11	332.43
017n	1.878E-11	1.952E-06	1.234E-08	23.50	c	0.1	12.04	3.918E+14	407.13
020n	1.985E-11	1.847E-06	1.446E-07	26.61	c	0.1	14.41	8.534E+15	531.35
021n	1.889E-11	1.941E-06	1.985E-07	28.15	c	0.1	14.50	1.402E+16	548.91
028n	1.937E-11	1.893E-06	3.840E-08	25.91	c	0.1	13.69	2.676E+16	534.42
029n	1.858E-11	1.973E-06	9.611E-09	24.05	c	0.1	12.19	1.196E+14	405.60
030n	1.947E-11	1.883E-06	7.591E-09	21.63	c	0.1	11.49	4.288E+14	407.98
032n	1.926E-11	1.904E-06	2.243E-09	26.06	c	0.1	13.69	7.088E+13	456.53
037n	1.913E-11	1.917E-06	2.617E-10	26.89	c	0.1	14.02	3.294E+15	506.77
127n	1.896E-11	1.934E-06	8.260E-10	26.89	c	0.1	13.90	2.116E+15	493.22
208n	1.846E-11	1.986E-06	1.009E-09	27.42	c	0.1	13.81	2.418E+15	495.25
004p	1.895E-11	1.935E-06	3.002E-08	22.48	c	0.1	11.62	5.894E+13	408.99
005p	1.914E-11	1.916E-06	3.451E-09	21.51	c	0.1	11.23	6.686E+14	430.38
013p	1.948E-11	1.882E-06	6.415E-10	26.74	c	0.1	14.21	1.035E+15	530.55
014p	2.009E-11	1.825E-06	6.660E-08	26.29	c	0.1	14.40	2.986E+19	676.95
015p	1.984E-11	1.848E-06	1.001E-10	20.99	c	0.1	11.36	7.429E+15	444.09
020p	2.028E-11	1.808E-06	3.400E-09	22.61	c	0.1	12.50	3.805E+54	1672.92
021p	1.941E-11	1.889E-06	1.899E-07	25.32	c	0.1	13.40	2.404E+16	604.24
028p	1.947E-11	1.883E-06	3.075E-08	22.60	c	0.1	12.00	1.961E+05	261.00
029p	1.856E-11	1.976E-06	2.993E-08	23.51	c	0.1	11.90	7.088E+15	476.17
030p	1.824E-11	2.010E-06	4.871E-09	23.35	c	0.1	11.62	2.279E+15	448.38
037p	1.916E-11	1.914E-06	2.951E-10	26.80	c	0.1	14.00	2.879E+16	556.31
042p	1.957E-11	1.874E-06	1.910E-08	26.24	c	0.1	14.00	3.997E+20	691.27
127p	1.886E-11	1.944E-06	1.227E-09	25.86	c	0.1	12.97	1.663E+15	513.20
208p	1.828E-11	2.006E-06	8.765E-10	26.68	c	0.1	13.34	1.808E+16	540.51

Table 26. Vendor A Voltage Ramp Data.

chip #	Cox (F)	Tox (cm)	Ipre (A)	Bkv (V)	Mode	Rate (MV/cm)	Field (MV/cm)	Afn	Bfn
007n	1.829E-11	2.005E-06	3.372E-09	26.07	c	1.0	13.0	7.284E+12	434.25
008n	1.860E-11	1.971E-06	1.545E-09	27.61	c	1.0	14.0	3.071E+13	443.48
010n	1.957E-11	1.874E-06	5.410E-10	26.18	c	1.0	14.0	4.618E+13	461.79
011n	1.905E-11	1.925E-06	2.766E-06	7.72	i	1.0	4.0	3.969E+08	134.47
019n	1.925E-11	1.905E-06	7.660E-10	25.57	c	1.0	13.4	7.013E+17	574.50
022n	1.911E-11	1.919E-06	2.450E-08	27.26	c	0.3	14.2	5.074E+11	412.77
023n	1.952E-11	1.878E-06	1.387E-07	26.32	c	1.0	14.0	1.966E+15	510.75
024n	1.945E-11	1.885E-06	1.445E-07	27.40	c	0.5	14.5	2.416E+11	409.44
025n	1.972E-11	1.859E-06	1.104E-07	26.04	c	1.0	14.0	1.530E+20	634.99
026n	2.002E-11	1.831E-06	1.465E-07	26.35	c	0.1	14.4	2.180E+16	546.61

Table 26. Vendor A Voltage Ramp Data (cont.).

chip #	Cox (F)	Tox (cm)	Ipre (A)	Bkv (V)	Mode	Rate (MV/cm)	Field (MV/cm)	Afn	Bfn
027n	1.951E-11	1.879E-06	1.847E-07	26.32	c	1.0	14.0	1.693E+17	583.25
033n	1.950E-11	1.880E-06	1.209E-09	26.33	c	0.5	14.0	1.785E+17	582.35
034n	1.846E-11	1.986E-06	1.786E-07	27.06	c	0.7	13.6	6.565E+13	470.13
035n	1.916E-11	1.914E-06	7.760E-10	27.75	c	0.5	14.5	2.402E+13	442.67
036n	1.968E-11	1.863E-06	7.180E-10	26.09	c	0.5	14.0	1.036E+12	420.30
037n	1.903E-11	1.927E-06	6.435E-10	24.96	c	0.5	13.0	1.023E+21	672.70
038n	1.927E-11	1.903E-06	7.348E-10	25.88	c	0.3	13.6	6.917E+12	427.01
039n	1.876E-11	1.954E-06	9.329E-10	26.39	c	0.5	13.5	6.156E+13	450.24
040n	1.938E-11	1.892E-06	1.053E-07	26.46	c	0.5	14.0	4.012E+16	538.42
041n	1.941E-11	1.889E-06	1.966E-07	26.46	c	0.5	14.0	1.943E+20	644.86
042n	1.972E-11	1.859E-06	1.753E-07	26.59	c	0.7	14.3	7.754E+14	487.74
129n	1.873E-11	1.958E-06	8.305E-10	26.63	c	0.3	13.6	2.801E+13	445.12
130n	1.870E-11	1.961E-06	1.565E-10	27.84	c	0.1	14.2	2.117E+12	429.61
134n	1.869E-11	1.962E-06	3.940E-10	26.68	c	0.7	13.6	1.943E+11	387.07
141n			9.866E-04		i				
144n	1.894E-11	1.936E-06	2.120E-10	26.33	c	0.7	13.6	1.388E+10	366.10
147n	1.932E-11	1.898E-06	5.965E-10	26.57	c	0.5	14.0	5.765E+14	483.33
204n	1.901E-11	1.929E-06	9.965E-10	26.23	c	0.7	13.6	1.661E+14	467.27
211n	1.843E-11	1.989E-06	1.023E-09	27.66	c	0.1	13.9	2.624E+12	424.45
215n	1.851E-11	1.981E-06	9.915E-10	26.74	c	0.5	13.5	9.632E+13	454.45
218n	1.930E-11	1.900E-06	9.425E-10	26.41	c	0.3	13.9	5.038E+12	424.93
222n	1.878E-11	1.952E-06	1.354E-09	27.34	c	0.5	14.0	3.539E+13	449.88
007p	1.829E-11	2.005E-06	2.424E-09	26.04	c	1.0	13.0	1.125E+11	411.39
009p	2.008E-11	1.826E-06	7.660E-10	25.48	c	1.0	14.0	7.023E+12	470.57
010p	1.965E-11	1.866E-06	1.840E-09	26.04	c	1.0	14.0	4.227E+14	524.57
011p	1.925E-11	1.905E-06	6.500E-12	26.74	c	1.0	14.0	1.782E+14	505.87
016p	1.875E-11	1.956E-06	1.792E-09	25.43	c	1.0	13.0	9.402E+11	431.49
018p	2.796E-11	1.312E-06	2.210E-10	28.86	m	1.0	22.0	2.309E+10	641.07
019p	1.830E-11	1.890E-06	4.195E-10	24.57	c	1.0	13.0	6.349E+13	391.70
022p	1.892E-11	1.938E-06	2.145E-08	27.54	c	0.3	14.2	1.114E+18	617.94
023p	1.944E-11	1.886E-06	1.973E-07	26.46	c	1.0	14.0	3.047E+17	612.60
024p	1.884E-11	1.946E-06	2.042E-07	26.32	c	0.5	14.5	1.583E+15	519.96
025p	1.972E-11	1.859E-06	1.958E-07	26.04	c	1.0	14.0	2.176E+13	475.09
026p	1.982E-11	1.850E-06	2.038E-07	26.45	c	0.1	14.3	5.021E+20	694.28
027p	1.915E-11	1.915E-06	1.305E-07	26.88	c	1.0	14.0	4.277E+09	349.21
032p	1.930E-11	1.900E-06	1.508E-09	24.70	c	1.0	13.0	4.567E+11	345.96
034p	1.870E-11	1.961E-06	5.735E-08	29.40	c	0.7	15.0	1.543E+17	621.10
035p	1.900E-11	1.930E-06	1.653E-10	27.02	c	0.5	14.0	4.069E+14	490.72
036p	1.905E-11	1.925E-06	6.293E-10	26.18	c	0.3	13.6	1.832E+14	481.99
037p	1.875E-11	1.956E-06	1.325E-09	26.89	c	0.5	13.5	1.266E+16	534.79
038p	1.939E-11	1.891E-06	1.314E-10	26.29	c	0.3	13.9	1.853E+15	520.88
039p	1.886E-11	1.944E-06	2.889E-10	27.22	c	0.5	14.0	1.256E+17	561.62
040p	1.968E-11	1.863E-06	1.776E-07	26.59	c	0.7	14.3	2.783E+19	671.71
041p	1.974E-11	1.857E-06	1.922E-07	26.04	c	0.5	14.0	2.531E+16	584.92
129p	1.888E-11	1.942E-06	5.465E-10	26.41	c	0.3	13.6	2.568E+15	518.61

Table 26. Vendor A Voltage Ramp Data (cont.).

chip #	Cox (F)	Tox (cm)	Ipre (A)	Bkv (V)	Mode	Rate (MV/cm)	Field (MV/cm)	Afn	Bfn
130p	1.864E-11	1.967E-06	5.640E-10	28.33	c	0.1	14.4	4.037E+13	487.01
134p	1.865E-11	1.966E-06	3.150E-10	26.74	c	0.7	13.6	1.539E+09	358.49
141p	1.878E-11	1.952E-06	8.170E-10	25.97	c	0.3	13.3	4.499E+10	395.92
144p	1.896E-11	1.934E-06	1.063E-09	26.30	c	0.7	13.6	7.056E+06	305.35
147p	1.953E-11	1.877E-06	1.048E-09	26.10	c	0.3	13.9	9.549E+10	415.05
204p	1.911E-11	1.919E-06	7.230E-10	27.44	c	0.7	14.3	3.973E+21	707.83
211p	1.815E-11	2.020E-06	1.355E-10	27.48	c	0.1	13.6	2.313E+14	492.81
215p	1.859E-11	1.972E-06	1.102E-09	26.63	c	0.5	13.5	3.303E+19	637.09
218p	1.919E-11	1.911E-06	1.116E-09	25.99	c	0.3	13.6	1.311E+13	454.79
222p	1.888E-11	1.942E-06	9.310E-10	27.19	c	0.5	14.0	8.651E+17	600.72

Table 27. Vendor B Fowler-Nordheim Data.

chip #	Cox (F)	Tox (cm)	Ipre (A)	Bkv (V)	Mode	Rate (MV/cm)	Field (MV/cm)	Afn	Bfn
05n1	2.341E-11	2.341E-06	8.401E-10	40.98	m	0.1	17.51	5.947E+12	602.56
08n1	2.467E-11	2.222E-06	4.535E-10	30.67	c	0.1	13.80	1.747E+08	351.95
13n1	2.485E-11	2.206E-06	1.045E-09	18.31	c	0.1	8.30	4.740E+02	107.22
16n1	2.456E-11	2.232E-06	1.094E-09	29.36	c	0.1	13.15	1.002E+08	304.07
32n1	2.372E-11	2.311E-06	3.792E-10	18.72	c	0.1	8.10	2.729E+03	106.62
35n1	2.491E-11	2.200E-06	1.603E-10	31.03	c	0.1	14.11	1.003E+08	345.81
47n1	2.399E-11	2.285E-06	8.651E-10	30.85	c	0.1	13.50	5.839E+07	327.81
48n1	2.416E-11	2.269E-06	8.643E-10	30.86	c	0.1	13.60	4.292E+07	323.87
49n1	2.427E-11	2.258E-06	1.215E-09	30.72	c	0.1	13.61	3.569E+07	322.91
50n1	2.415E-11	2.270E-06	1.313E-09	29.74	c	0.1	13.10	2.255E+07	282.10
53n1	2.408E-11	2.276E-06	8.278E-10	40.98	m	0.1	18.01	2.202E+12	610.66
54n1	2.466E-11	2.223E-06	1.456E-10	31.35	c	0.1	14.10	2.052E+08	355.18
01p1	2.435E-11	2.251E-06	3.505E-11	30.62	c	0.1	13.60	1.931E+07	297.19
02p1	2.431E-11	2.255E-06	6.062E-10	30.67	c	0.1	13.60	1.917E+07	297.71
03p1	2.427E-11	2.258E-06	8.005E-10	29.42	c	0.1	13.03	9.331E+07	313.01
05p1	2.398E-11	2.286E-06	7.965E-10	34.00	c	0.1	14.87	2.244E+12	617.74
08p1	2.421E-11	2.264E-06	3.418E-10	30.80	c	0.1	13.60	1.606E+07	296.19
13p1	2.424E-11	2.261E-06	1.059E-09	19.22	c	0.1	8.50	3.652E+02	88.48
32p1	2.427E-11	2.259E-06	8.005E-10	19.20	c	0.1	8.50	5.397E+02	89.73
35p1	2.446E-11	2.241E-06	2.265E-10	30.71	c	0.1	13.70	1.649E+07	296.64
47p1	2.352E-11	2.330E-06	8.367E-10	30.77	c	0.1	13.21	3.584E+07	295.82
48p1	2.371E-11	2.312E-06	8.460E-10	30.52	c	0.1	13.20	7.334E+07	305.09
49p1	2.386E-11	2.297E-06	1.253E-09	20.68	c	0.1	9.00	4.057E+03	96.87
50p1	2.375E-11	2.308E-06	5.436E-10	22.22	c	0.1	9.63	3.097E+03	98.45
53p1	2.365E-11	2.318E-06	7.417E-10	29.00	c	0.1	12.51	3.567E+07	304.76
54p1	2.418E-11	2.282E-06	1.715E-10	30.83	c	0.1	14.51	2.037E+07	298.83

Table 28. Vendor B Voltage Ramp Data.

chip #	Cox (F)	Tox (cm)	Ipre (A)	Bkv (V)	Mode	Rate (MV/cm)	Field (MV/cm)	Afn	Bfn
06n1	2.447E-11	2.240E-06	2.481E-10	29.12	c	1.0	13.0	3.572E+10	398.33
07n1	2.444E-11	2.243E-06	3.008E-10	29.16	c	1.0	13.0	2.353E+10	393.92
11n1	2.474E-11	2.217E-06	1.173E-10	30.15	c	0.1	13.6	1.543E+08	347.80
12n1	2.468E-11	2.221E-06	6.579E-10	28.87	c	1.0	13.0	3.423E+10	399.98
14n1	2.450E-11	2.237E-06	7.067E-10	29.08	c	1.0	13.0	1.248E+06	290.28
15n1	2.434E-11	2.252E-06	5.300E-10	29.28	c	1.0	13.0	5.938E+09	377.08
16n1	2.427E-11	2.258E-06	1.201E-10	29.35	c	1.0	13.0	2.157E+11	403.58
17n1	2.488E-11	2.203E-06	2.859E-10	28.64	c	1.0	13.0	5.223E+10	406.59
18n1	2.510E-11	2.184E-06	2.920E-10	28.39	c	1.0	13.0	5.468E+10	411.20
19n1	2.502E-11	2.191E-06	5.314E-10	28.48	c	1.0	13.0	5.588E+06	311.37
20n1	2.491E-11	2.200E-06	3.546E-10	29.70	c	0.5	13.5	2.623E+07	328.99
21n1	2.484E-11	2.207E-06	4.443E-10	28.69	c	1.0	13.0	1.527E+09	379.65
23n1	2.462E-11	2.226E-06	4.557E-10	30.05	c	0.5	13.5	1.402E+08	341.02
24n1	2.525E-11	2.171E-06	5.493E-10	28.22	c	1.0	13.0	9.985E+08	362.87
25n1	2.487E-11	2.204E-06	1.449E-10	28.65	c	1.0	13.0	6.287E+09	380.20
26n1	2.514E-11	2.180E-06	5.799E-10	29.43	c	0.5	13.5	9.455E+06	318.84
27n1	2.475E-11	2.215E-06	6.815E-10	28.79	c	1.0	13.0	3.524E+08	357.05
28n1	2.463E-11	2.225E-06	1.253E-09	28.93	c	1.0	13.0	4.389E+07	328.93
29n1	2.455E-11	2.233E-06	1.220E-09	29.03	c	1.0	13.0	3.363E+07	329.73
30n1	2.471E-11	2.218E-06	5.612E-10	28.83	c	1.0	13.0	2.322E+10	399.25
31n1	2.459E-11	2.229E-06	5.580E-10	28.98	c	1.0	13.0	3.635E+09	375.64
33n1	2.483E-11	2.207E-06	4.255E-10	28.69	c	1.0	13.0	7.468E+10	410.80
34n1	2.507E-11	2.186E-06	1.600E-10	29.51	c	0.5	13.5	1.148E+09	378.10
36n1	2.464E-11	2.224E-06	4.320E-10	28.91	c	1.0	13.0	5.077E+07	311.14
37n1	2.454E-11	2.233E-06	3.035E-10	29.04	c	1.0	13.0	4.836E+07	330.28
38n1	2.448E-11	2.239E-06	9.250E-11	30.45	c	0.1	13.6	1.207E+08	344.30
39n1	2.436E-11	2.250E-06	6.390E-10	30.38	c	0.5	13.5	2.558E+08	353.69
40n1	2.474E-11	2.215E-06	3.747E-10	28.80	c	1.0	13.0	4.316E+10	403.99
41n1	2.502E-11	2.191E-06	5.769E-10	29.58	c	0.5	13.5	1.325E+08	350.89
42n1	2.466E-11	2.223E-06	1.078E-09	30.01	c	0.5	13.5	8.010E+07	336.36
43n1	2.463E-11	2.225E-06	1.243E-09	28.93	c	1.0	13.0	3.864E+10	401.67
44n1	2.448E-11	2.239E-06	6.700E-10	29.11	c	1.0	13.0	2.252E+10	393.94
45n1	2.439E-11	2.247E-06	1.895E-10	30.34	c	0.5	13.5	2.023E+09	378.95
46n1	2.428E-11	2.257E-06	1.273E-09	29.35	c	1.0	13.0	2.638E+09	367.46
51n1	2.405E-11	2.279E-06	5.540E-10	41.02	m	0.5	18.0	5.189E+13	664.21
52n1	2.393E-11	2.290E-06	7.899E-10	30.92	c	0.5	13.5	8.901E+10	415.76
01n2	2.482E-11	2.208E-06	1.238E-09	28.71	c	0.5	13.0	5.208E+07	333.89
02n2	2.463E-11	2.225E-06	8.225E-10	28.93	c	1.0	13.0	3.980E+09	372.70
03n2	2.507E-11	2.180E-06	1.530E-10	28.42	c	1.0	13.0	6.876E+09	383.51
04n2	2.483E-11	2.207E-06	4.390E-10	28.70	c	0.5	13.0	1.115E+08	340.67
05n2	2.471E-11	2.218E-06	1.608E-09	28.82	c	1.0	13.0	7.903E+10	407.72
06n2	2.479E-11	2.211E-06	6.425E-10	29.85	c	0.5	13.5	2.103E+07	323.65
07n2	2.469E-11	2.220E-06	1.177E-09	29.97	c	0.1	13.3	1.612E+08	347.44
08n2	2.460E-11	2.228E-06	1.418E-09	30.08	c	0.5	13.5	2.526E+07	325.89
09n2	2.511E-11	2.183E-06	1.503E-09	28.38	c	1.0	13.0	8.639E+07	335.48

Table 28. Vendor B Voltage Ramp Data (cont.).

chip #	Cox (F)	Tox (cm)	Ipre (A)	Bkv (V)	Mode	Rate (MV/cm)	Field (MV/cm)	Afn	Bfn
10n2	2.487E-11	2.204E-06	3.450E-10	29.75	c	0.5	13.5	8.565E+07	334.84
11n2	2.482E-11	2.208E-06	8.375E-10	28.71	c	1.0	13.0	5.454E+07	330.38
12n2	2.483E-11	2.207E-06	9.600E-10	29.80	c	0.5	13.5	4.733E+07	331.02
13n2	2.447E-11	2.240E-06	1.660E-10	29.12	c	0.5	13.0	5.811E+07	330.25
14n2	2.440E-11	2.246E-06	1.295E-09	30.33	c	0.5	13.5	5.002E+07	329.77
15n2	2.419E-11	2.266E-06	1.220E-10	30.59	c	0.5	13.5	5.249E+07	330.25
16n2	2.522E-11	2.173E-06	6.005E-10	29.34	c	0.5	13.5	2.367E+09	377.51
17n2	2.498E-11	2.194E-06	1.100E-10	28.53	c	1.0	13.0	8.485E+07	333.54
18n2	2.483E-11	2.207E-06	3.415E-10	28.70	c	1.0	13.0	6.598E+07	331.07
19n2	2.472E-11	2.217E-06	1.250E-10	28.33	c	1.0	13.0	5.689E+07	329.09
20n2	2.471E-11	2.218E-06	8.410E-10	30.17	c	0.1	13.6	2.577E+08	349.65
21n2	2.461E-11	2.227E-06	1.495E-10	30.07	c	0.5	13.5	4.626E+07	329.96
22n2	2.435E-11	2.251E-06	1.369E-09	30.39	c	0.5	13.5	5.296E+07	330.03
23n2	2.419E-11	2.266E-06	3.185E-10	27.19	c	0.5	12.0	3.502E+07	329.73
24n2	2.517E-11	2.178E-06	6.765E-10	28.31	c	1.0	13.0	1.355E+08	341.44
25n2	2.503E-11	2.190E-06	7.485E-10	28.47	c	1.0	13.0	8.483E+07	334.59
26n2	2.483E-11	2.207E-06	6.825E-10	28.70	c	1.0	13.0	6.637E+07	331.31
27n2	2.474E-11	2.215E-06	9.185E-10	26.59	c	1.0	12.0	9.522E+08	359.80
28n2	2.484E-11	2.207E-06	1.491E-09	22.07	c	1.0	10.0	1.494E+61	1564.67
29n2	2.445E-11	2.242E-06	7.775E-10	29.14	c	1.0	13.0	4.483E+07	327.14
30n2	2.432E-11	2.254E-06	1.475E-10	30.43	c	0.5	13.5	4.735E+07	328.37
31n2	2.415E-11	2.270E-06	6.995E-10	23.83	c	0.5	10.5	4.037E+03	103.59
32n2	2.517E-11	2.178E-06	1.135E-09	28.31	c	1.0	13.0	8.587E+07	336.99
33n2	2.501E-11	2.191E-06	1.316E-09	28.49	c	1.0	13.0	8.500E+07	334.44
34n2	2.476E-11	2.214E-06	9.200E-10	28.78	c	1.0	13.0	7.720E+07	332.09
35n2	2.466E-11	2.223E-06	1.423E-09	26.67	c	1.0	12.0	4.655E+06	306.88
36n2	2.485E-11	2.206E-06	6.570E-10	28.67	c	1.0	13.0	4.210E+07	330.48
37n2	2.460E-11	2.228E-06	1.531E-09	28.97	c	1.0	13.0	3.420E+07	326.50
38n2	2.431E-11	2.255E-06	1.545E-10	30.44	c	0.5	13.5	5.943E+07	331.48
39n2	2.407E-11	2.277E-06	8.710E-10	30.74	c	0.5	13.5	6.880E+07	331.82
40n2	2.481E-11	2.209E-06	4.535E-10	29.38	c	0.1	13.3	9.441E+08	362.63
41n2	2.480E-11	2.210E-06	1.279E-09	28.73	c	0.5	13.0	9.835E+07	336.60
42n2	2.480E-11	2.210E-06	6.455E-10	27.63	c	0.5	12.5	1.757E+08	348.19
43n2	2.458E-11	2.230E-06	8.890E-10	30.10	c	0.5	13.5	7.891E+07	333.87
44n2	2.437E-11	2.249E-06	1.295E-09	30.14	c	0.1	13.4	5.831E+08	357.04
45n2	2.427E-11	2.258E-06	7.985E-10	29.36	c	1.0	13.0	5.793E+07	330.51
47n2	2.434E-11	2.252E-06	7.605E-10	27.02	c	1.0	12.0	2.696E+09	371.32
46n2	2.406E-11	2.278E-06	1.300E-09	30.76	c	0.5	13.5	7.324E+07	332.52
48n2	2.464E-11	2.224E-06	1.143E-09	26.69	c	1.0	12.0	9.364E+04	260.74
49n2	2.465E-11	2.224E-06	1.138E-09	26.68	c	1.0	12.0	3.968E+06	306.76
50n2	2.450E-11	2.237E-06	1.313E-09	29.08	c	1.0	13.0	7.600E+07	333.34
51n2	2.437E-11	2.249E-06	6.720E-10	29.24	c	1.0	13.0	8.241E+07	334.77
52n2	2.453E-11	2.234E-06	6.285E-10	30.17	c	0.5	13.5	4.542E+07	332.69
53n2	2.453E-11	2.234E-06	1.048E-09	29.05	c	1.0	13.0	1.070E+08	337.47
54n2	2.436E-11	2.250E-06	9.170E-10	29.25	c	1.0	13.0	1.185E+08	337.47

Table 28. Vendor B Voltage Ramp Data (cont.).

chip #	Cox (F)	Tox (cm)	Ipre (A)	Bkv (V)	Mode	Rate (MV/cm)	Field (MV/cm)	Afn	Bfn
04p1	2.419E-11	2.266E-06	6.274E-10	29.46	c	0.5	13.0	1.550E+07	291.60
06p1	2.399E-11	2.285E-06	4.607E-10	29.71	c	1.0	13.0	1.005E+07	290.88
07p1	2.393E-11	2.290E-06	6.660E-10	29.77	c	1.0	13.0	1.985E+09	339.36
10p1	2.426E-11	2.259E-06	6.688E-10	29.37	c	1.0	13.0	2.729E+09	344.90
11p1	2.421E-11	2.264E-06	1.457E-10	29.66	c	0.1	13.1	1.152E+07	289.92
12p1	2.421E-11	2.264E-06	5.467E-10	29.43	c	1.0	13.0	1.020E+06	266.86
14p1	2.403E-11	2.281E-06	1.690E-10	29.66	c	1.0	13.0	2.808E+05	321.16
15p1	2.390E-11	2.293E-06	6.717E-10	29.81	c	1.0	13.0	2.378E+09	343.14
17p1	2.432E-11	2.254E-06	5.393E-10	29.30	c	1.0	13.0	3.248E+09	346.79
18p1	2.455E-11	2.233E-06	4.527E-10	29.03	c	1.0	13.0	2.054E+09	344.99
19p1	2.449E-11	2.238E-06	4.228E-10	29.29	c	1.0	13.0	2.462E+08	318.29
20p1	2.439E-11	2.247E-06	5.315E-10	29.21	c	0.5	13.0	6.330E+06	284.80
21p1	2.433E-11	2.253E-06	4.105E-10	29.29	c	1.0	13.0	2.311E+08	317.72
22p1	2.427E-11	2.258E-06	1.537E-10	30.03	c	0.1	13.3	9.790E+06	291.62
23p1	2.413E-11	2.271E-06	5.263E-10	29.52	c	0.5	13.0	4.338E+07	309.14
24p1	2.438E-11	2.248E-06	5.008E-10	29.23	c	1.0	13.0	3.111E+09	346.22
25p1	2.415E-11	2.270E-06	3.361E-10	29.51	c	1.0	13.0	2.363E+09	339.85
26p1	2.463E-11	2.225E-06	2.028E-10	30.04	c	0.5	13.5	9.079E+06	291.23
27p1	2.422E-11	2.263E-06	1.022E-09	29.42	c	1.0	13.0	2.922E+06	269.38
28p1	2.414E-11	2.270E-06	1.239E-09	29.51	c	1.0	13.0	1.163E+07	287.06
29p1	2.409E-11	2.275E-06	7.600E-10	29.58	c	1.0	13.0	2.113E+09	342.02
30p1	2.391E-11	2.292E-06	1.247E-09	29.80	c	1.0	13.0	2.726E+08	315.08
31p1	2.412E-11	2.272E-06	1.425E-10	29.54	c	1.0	13.0	5.742E+05	263.26
33p1	2.434E-11	2.252E-06	1.944E-10	29.28	c	1.0	13.0	3.126E+08	318.11
34p1	2.453E-11	2.234E-06	2.507E-10	29.04	c	0.5	13.0	6.025E+06	285.07
36p1	2.416E-11	2.269E-06	6.765E-10	29.50	c	1.0	13.0	8.713E+09	359.55
37p1	2.405E-11	2.279E-06	1.111E-09	29.63	c	1.0	13.0	1.091E+07	286.47
38p1	2.400E-11	2.284E-06	7.050E-10	30.15	c	0.1	13.2	9.898E+06	288.44
39p1	2.390E-11	2.293E-06	1.001E-09	29.81	c	0.5	13.0	1.544E+07	293.72
40p1	2.424E-11	2.261E-06	4.674E-10	29.39	c	1.0	13.0	6.723E+08	327.34
41p1	2.449E-11	2.238E-06	3.618E-10	30.21	c	0.5	13.5	5.635E+07	312.82
42p1	2.414E-11	2.270E-06	2.215E-10	29.52	c	0.5	13.0	1.612E+07	290.22
43p1	2.413E-11	2.271E-06	4.590E-10	29.53	c	0.5	13.0	1.321E+07	288.64
45p1	2.394E-11	2.289E-06	1.223E-09	29.76	c	0.5	13.0	1.613E+07	293.81
46p1	2.386E-11	2.297E-06	7.500E-10	29.86	c	1.0	13.0	5.160E+09	353.75
51p1	2.361E-11	2.321E-06	7.529E-10	33.65	c	0.5	14.5	6.456E+08	350.16
52p1	2.349E-11	2.333E-06	7.375E-10	30.33	c	0.5	13.0	1.013E+07	311.92
01p2	2.430E-11	2.256E-06	5.315E-10	29.32	c	0.5	13.0	1.446E+07	291.34
02p2	2.412E-11	2.272E-06	4.190E-10	29.54	c	1.0	13.0	4.787E+07	300.18
03p2	2.455E-11	2.233E-06	1.355E-09	29.02	c	1.0	13.0	1.443E+09	333.26
04p2	2.431E-11	2.255E-06	8.750E-11	29.31	c	0.5	13.0	1.897E+07	292.44
05p2	2.417E-11	2.286E-06	8.030E-10	29.48	c	1.0	13.0	1.029E+07	289.12
06p2	2.430E-11	2.256E-06	3.395E-10	29.32	c	0.5	13.0	2.422E+07	299.58
07p2	2.392E-11	2.291E-06	1.512E-09	27.96	c	0.1	12.2	4.082E+06	277.64
08p2	2.392E-11	2.291E-06	4.765E-10	29.79	c	0.5	13.0	9.428E+06	285.04

Table 28. Vendor B Voltage Ramp Data (cont.)

chip #	Cox (F)	Tox (cm)	Ipre (A)	Bkv (V)	Mode	Rate (MV/cm)	Field (MV/cm)	Afn	Bfn
09p2	2.444E-11	2.243E-06	6.215E-10	29.16	c	1.0	13.0	1.917E+07	288.16
10p2	2.425E-11	2.260E-06	1.360E-09	29.38	c	0.5	13.0	2.286E+07	290.61
11p2	2.421E-11	2.264E-06	1.082E-09	29.43	c	1.0	13.0	1.432E+07	286.47
12p2	2.434E-11	2.252E-06	4.480E-10	29.28	c	0.5	13.0	8.856E+06	284.77
13p2	2.388E-11	2.295E-06	1.365E-10	29.84	c	0.5	13.0	1.716E+07	288.16
14p2	2.396E-11	2.288E-06	3.500E-11	29.74	c	0.5	13.0	1.014E+07	285.27
15p2	2.363E-11	2.320E-06	7.290E-10	30.16	c	0.5	13.0	1.442E+07	287.39
16p2	2.462E-11	2.266E-06	1.083E-09	28.94	c	0.5	13.0	1.642E+07	288.78
17p2	2.427E-11	2.258E-06	4.690E-10	29.36	c	1.0	13.0	2.907E+07	291.01
18p2	2.434E-11	2.252E-06	8.950E-10	27.02	c	1.0	12.0	1.126E+09	335.27
19p2	2.424E-11	2.261E-06	1.111E-11	29.40	c	1.0	13.0	1.269E+07	285.42
20p2	2.410E-11	2.274E-06	1.412E-09	29.57	c	0.1	13.0	8.767E+08	334.41
21p2	2.391E-11	2.292E-06	1.045E-09	29.80	c	0.5	13.0	1.580E+07	287.78
22p2	2.386E-11	2.297E-06	1.063E-09	28.72	c	0.5	12.5	1.757E+07	293.50
23p2	2.354E-11	2.328E-06	1.286E-09	30.27	c	0.5	13.0	1.924E+07	289.17
24p2	2.458E-11	2.230E-06	5.425E-10	28.99	c	1.0	13.0	4.444E+06	278.35
25p2	2.444E-11	2.243E-06	1.370E-09	23.55	c	0.5	10.5	4.278E+08	318.58
26p2	2.426E-11	2.259E-06	1.042E-09	29.37	c	1.0	13.0	1.648E+07	287.37
27p2	2.422E-11	2.263E-06	9.255E-10	29.42	c	0.1	13.0	1.685E+07	291.10
28p2	2.435E-11	2.251E-06	1.084E-09	29.26	c	1.0	13.0	7.601E+06	283.34
29p2	2.383E-11	2.300E-06	1.434E-09	29.90	c	1.0	13.0	1.559E+07	286.75
30p2	2.383E-11	2.300E-06	1.016E-09	29.90	c	0.5	13.0	1.270E+07	286.89
31p2	2.363E-11	2.320E-06	8.000E-11	30.17	c	0.5	13.0	1.485E+07	287.83
32p2	2.456E-11	2.232E-06	1.121E-09	29.01	c	1.0	13.0	1.618E+07	288.30
33p2	2.450E-11	2.237E-06	7.285E-10	29.08	c	1.0	13.0	1.502E+07	286.86
34p2	2.422E-11	2.263E-06	1.384E-09	29.42	c	1.0	13.0	1.831E+07	287.93
35p2	2.420E-11	2.265E-06	7.495E-10	29.44	c	1.0	13.0	1.452E+07	286.55
36p2	2.408E-11	2.276E-06	1.046E-09	29.59	c	1.0	13.0	1.262E+07	285.43
38p2	2.370E-11	2.313E-06	5.500E-11	30.07	c	0.5	13.0	1.743E+07	288.70
37p2	2.375E-11	2.308E-06	1.367E-09	30.00	c	1.0	13.0	1.702E+07	286.96
39p2	2.373E-11	2.310E-06	1.332E-09	30.03	c	0.5	13.0	1.106E+07	286.10
40p2	2.434E-11	2.252E-06	1.178E-09	29.50	c	0.1	13.1	1.621E+09	340.00
41p2	2.415E-11	2.270E-06	2.980E-10	29.51	c	0.5	13.0	2.735E+07	292.04
42p2	2.408E-11	2.276E-06	7.790E-10	29.59	c	0.5	13.0	2.340E+07	290.63
43p2	2.393E-11	2.290E-06	4.550E-11	29.78	c	0.5	13.0	2.389E+07	290.74
44p2	2.385E-11	2.298E-06	1.565E-10	29.88	c	0.5	13.0	1.901E+07	289.14
45p2	2.367E-11	2.316E-06	9.110E-10	30.10	c	1.0	13.0	1.671E+07	287.73
47p2	2.384E-11	2.299E-06	5.060E-10	29.89	c	1.0	13.0	2.668E+07	291.64
46p2	2.346E-11	2.336E-06	1.880E-10	30.37	c	0.5	13.0	2.413E+07	291.22
48p2	2.408E-11	2.276E-06	7.735E-10	29.59	c	0.5	13.0	2.584E+07	291.78
49p2	2.419E-11	2.266E-06	2.585E-10	29.46	c	1.0	13.0	1.337E+07	286.70
50p2	2.395E-11	2.289E-06	7.335E-10	29.75	c	1.0	13.0	1.636E+07	287.63
51p2	2.358E-11	2.324E-06	1.111E-09	27.89	c	1.0	12.0	9.663E+07	303.04
52p2	2.379E-11	2.304E-06	1.238E-09	29.95	c	1.0	13.0	1.134E+07	285.68
53p2	2.408E-11	2.276E-06	9.535E-10	29.59	c	0.5	13.0	1.795E+07	289.60
54p2	2.402E-11	2.282E-06	5.995E-10	29.67	c	1.0	13.0	1.357E+07	287.33

APPENDIX D: STATISTICAL DATA ANALYSIS

Table 29. Uncensored Vendor A Capacitance Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	19.14	19.10	19.18	18.96	19.19	19.13
	Standard Error	0.11	0.13	0.11	0.21	0.18	0.06
	Median	19.14	19.19	19.32	18.94	19.38	19.15
	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	18.94
	Standard Deviation	0.47	0.26	0.37	0.48	0.51	0.43
	Variance	0.22	0.07	0.13	0.23	0.26	0.18
	Kurtosis	-0.73	1.76	-0.71	1.73	-0.34	-0.80
	Skewness	0.24	-1.46	-0.60	1.10	-0.95	-0.09
	Range	1.59	0.57	1.17	1.26	1.43	1.73
	Minimum	18.43	18.73	18.51	18.46	18.29	18.29
	Maximum	20.02	19.30	19.68	19.72	19.72	20.02
	Sum	344.46	76.41	210.98	94.82	153.51	880.18
	Count	18.00	4.00	11.00	5.00	8.00	46.00
P	Mean	19.17	19.11	18.95	19.02	19.99	19.30
	Standard Error	0.16	0.10	0.14	0.19	0.81	0.20
	Median	19.16	19.05	18.86	18.96	19.30	19.11
	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	18.86
	Standard Deviation	0.65	0.28	0.37	0.41	2.70	1.39
	Variance	0.43	0.08	0.14	0.17	7.30	1.93
	Kurtosis	-1.00	-1.16	4.70	1.29	9.77	34.10
	Skewness	-0.05	0.52	1.99	1.20	3.05	5.43
	Range	2.13	0.75	1.15	1.03	9.67	9.81
	Minimum	18.15	18.78	18.59	18.65	18.29	18.15
	Maximum	20.28	19.53	19.74	19.68	27.96	27.96
	Sum	325.94	133.74	132.66	95.10	219.89	907.33
	Count	17.00	7.00	7.00	5.00	11.00	47.00
ALL	Mean	19.15	19.10	19.09	18.99	19.65	19.22
	Standard Error	0.09	0.08	0.09	0.13	0.48	0.11
	Median	19.14	19.11	19.02	18.95	19.30	19.14
	Mode	19.14	#N/A	#N/A	#N/A	18.29	18.78
	Standard Deviation	0.56	0.26	0.38	0.42	2.08	1.03
	Variance	0.31	0.07	0.14	0.18	4.32	1.06
	Kurtosis	-0.75	-1.04	-1.14	-0.08	16.25	57.03
	Skewness	0.06	0.06	0.24	0.87	3.89	6.72
	Range	2.13	0.80	1.23	1.26	9.67	9.81
	Minimum	18.15	18.73	18.51	18.46	18.29	18.15
	Maximum	20.28	19.53	19.74	19.72	27.96	27.96
	Sum	670.40	210.15	343.64	189.92	373.40	1787.51
	Count	35.00	11.00	18.00	10.00	19.00	93.00

Table 30. Censored Vendor A Capacitance Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	19.14	19.10	19.18	18.96	19.21	19.14
	Standard Error	0.11	0.13	0.11	0.21	0.21	0.06
	Median	19.14	19.19	19.32	18.94	19.51	19.16
	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	18.94
	Standard Deviation	0.47	0.26	0.37	0.48	0.55	0.43
	Variance	0.22	0.07	0.13	0.23	0.30	0.19
	Kurtosis	-0.73	1.76	-0.71	1.73	-0.44	-0.85
	Skewness	0.24	-1.46	-0.60	1.10	-1.09	-0.10
	Range	1.59	0.57	1.17	1.26	1.43	1.73
	Minimum	18.43	18.73	18.51	18.46	18.29	18.29
	Maximum	20.02	19.30	19.68	19.72	19.72	20.02
	Sum	344.46	76.41	210.98	94.82	134.46	861.13
	Count	18.00	4.00	11.00	5.00	7.00	45.00
P	Mean	19.17	19.11	18.95	19.02	19.19	19.12
	Standard Error	0.16	0.10	0.14	0.19	0.19	0.08
	Median	19.16	19.05	18.86	18.96	19.28	19.08
	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	18.86
	Standard Deviation	0.65	0.28	0.37	0.41	0.59	0.52
	Variance	0.43	0.08	0.14	0.17	0.35	0.27
	Kurtosis	-1.00	-1.16	4.70	1.29	-0.65	-0.52
	Skewness	-0.05	0.52	1.99	1.20	-0.39	0.18
	Range	2.13	0.75	1.15	1.03	1.79	2.13
	Minimum	18.15	18.78	18.59	18.65	18.29	18.15
	Maximum	20.28	19.53	19.74	19.68	20.08	20.28
	Sum	325.94	133.74	132.66	95.10	191.93	879.37
	Count	17.00	7.00	7.00	5.00	10.00	46.00
ALL	Mean	19.15	19.10	19.09	18.99	19.20	19.13
	Standard Error	0.09	0.08	0.09	0.13	0.13	0.05
	Median	19.14	19.11	19.02	18.95	19.30	19.14
	Mode	19.14	#N/A	#N/A	#N/A	18.29	18.78
	Standard Deviation	0.56	0.26	0.38	0.42	0.56	0.48
	Variance	0.31	0.07	0.14	0.18	0.31	0.23
	Kurtosis	-0.75	-1.04	-1.14	-0.08	-0.79	-0.58
	Skewness	0.06	0.06	0.24	0.87	-0.56	0.07
	Range	2.13	0.80	1.23	1.26	1.79	2.13
	Minimum	18.15	18.73	18.51	18.46	18.29	18.15
	Maximum	20.28	19.53	19.74	19.72	20.08	20.28
	Sum	670.40	210.15	343.64	189.92	326.39	1740.50
	Count	35.00	11.00	18.00	10.00	17.00	91.00

Table 31. Uncensored Vendor A Oxide Thickness Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	191.70	192.00	191.23	193.44	191.20	191.72
N	Standard Error	1.10	1.33	1.11	2.14	1.83	0.63
N	Median	191.65	191.10	189.80	193.60	189.20	191.50
N	Mode	186.70	#N/A	#N/A	#N/A	#N/A	193.60
N	Standard Deviation	4.65	2.67	3.69	4.78	5.19	4.28
N	Variance	21.61	7.11	13.63	22.85	26.92	18.33
N	Kurtosis	-0.77	1.84	-0.62	1.57	-0.20	-0.80
N	Skewness	-0.17	1.47	0.65	-1.03	1.00	0.15
N	Range	15.80	5.80	11.80	12.70	14.60	17.40
N	Minimum	183.10	190.00	186.30	185.90	185.90	183.10
N	Maximum	198.90	195.80	198.10	198.60	200.50	200.50
N	Sum	3450.60	768.00	2103.50	967.20	1529.60	8818.90
N	Count	18.00	4.00	11.00	5.00	8.00	46.00
P	Mean	191.45	191.94	193.53	192.86	184.73	190.41
P	Standard Error	1.59	1.05	1.39	1.85	5.54	1.48
P	Median	191.40	192.50	194.40	193.40	189.00	191.60
P	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	194.40
P	Standard Deviation	6.55	2.78	3.69	4.15	18.39	10.17
P	Variance	42.96	7.71	13.62	17.18	338.18	103.35
P	Kurtosis	-1.02	-1.16	4.56	1.14	9.12	25.49
P	Skewness	0.15	-0.52	-1.95	-1.15	-2.90	-4.39
P	Range	21.20	7.50	11.50	10.30	69.30	70.80
P	Minimum	180.80	187.70	185.70	186.30	131.20	131.20
P	Maximum	202.00	195.20	197.20	196.60	200.50	202.00
P	Sum	3254.70	1343.60	1354.70	964.30	2032.00	8949.30
P	Count	17.00	7.00	7.00	5.00	11.00	47.00
ALL	Mean	191.58	191.96	192.12	193.15	187.45	191.06
ALL	Standard Error	0.94	0.78	0.89	1.34	3.32	0.81
ALL	Median	191.60	191.90	192.85	193.50	189.00	191.60
ALL	Mode	191.60	#N/A	#N/A	#N/A	200.50	195.20
ALL	Standard Deviation	5.57	2.60	3.76	4.23	14.46	7.81
ALL	Variance	31.03	6.76	14.16	17.89	209.13	61.07
ALL	Kurtosis	-0.77	-1.02	-1.15	-0.14	14.33	37.18
ALL	Skewness	0.04	-0.04	-0.20	-0.82	-3.53	-4.89
ALL	Range	21.20	8.10	12.40	12.70	69.30	70.80
ALL	Minimum	180.80	187.70	185.70	185.90	131.20	131.20
ALL	Maximum	202.00	195.80	198.10	198.60	200.50	202.00
ALL	Sum	6705.30	2111.60	3458.20	1931.50	3561.60	17768.20
ALL	Count	35.00	11.00	18.00	10.00	19.00	93.00

Table 32. Censored Vendor A Oxide Thickness Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	191.70	192.00	191.23	193.44	191.01	191.70
	Standard Error	1.10	1.33	1.11	2.14	2.11	0.65
	Median	191.65	191.10	189.80	193.60	187.90	191.40
	Mode	186.70	#N/A	#N/A	#N/A	#N/A	193.60
	Standard Deviation	4.65	2.67	3.69	4.78	5.58	4.33
	Variance	21.61	7.11	13.63	22.85	31.09	18.73
	Kurtosis	-0.77	1.84	-0.62	1.57	-0.32	-0.84
	Skewness	-0.17	1.47	0.65	-1.03	1.12	0.17
	Range	15.80	5.80	11.80	12.70	14.60	17.40
	Minimum	183.10	190.00	186.30	185.90	185.90	183.10
	Maximum	198.90	195.80	198.10	198.60	200.50	200.50
	Sum	3450.60	768.00	2103.50	967.20	1337.10	8626.40
	Count	18.00	4.00	11.00	5.00	7.00	45.00
P	Mean	191.45	191.94	193.53	192.86	190.08	191.70
	Standard Error	1.59	1.05	1.39	1.85	1.60	0.75
	Median	191.40	192.50	194.40	193.40	189.50	191.75
	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	194.40
	Standard Deviation	6.55	2.78	3.69	4.15	5.06	5.10
	Variance	42.96	7.71	13.62	17.18	25.57	26.04
	Kurtosis	-1.02	-1.16	4.56	1.14	1.10	-0.47
	Skewness	0.15	-0.52	-1.95	-1.15	0.82	-0.04
	Range	21.20	7.50	11.50	10.30	17.90	21.20
	Minimum	180.80	187.70	185.70	186.30	182.60	180.80
	Maximum	202.00	195.20	197.20	196.60	200.50	202.00
	Sum	3254.70	1343.60	1354.70	964.30	1900.80	8818.10
	Count	17.00	7.00	7.00	5.00	10.00	46.00
ALL	Mean	191.58	191.96	192.12	193.15	190.46	191.70
	Standard Error	0.94	0.78	0.89	1.34	1.24	0.49
	Median	191.60	191.90	192.85	193.50	189.00	191.60
	Mode	191.60	#N/A	#N/A	#N/A	200.50	195.20
	Standard Deviation	5.57	2.60	3.76	4.23	5.13	4.71
	Variance	31.03	6.76	14.16	17.89	26.27	22.18
	Kurtosis	-0.77	-1.02	-1.15	-0.14	0.04	-0.56
	Skewness	0.04	-0.04	-0.20	-0.82	0.86	0.04
	Range	21.20	8.10	12.40	12.70	17.90	21.20
	Minimum	180.80	187.70	185.70	185.90	182.60	180.80
	Maximum	202.00	195.80	198.10	198.60	200.50	202.00
	Sum	6705.30	2111.60	3458.20	1931.50	3237.90	17444.50
	Count	35.00	11.00	18.00	10.00	17.00	91.00

Table 33. Uncensored Vendor A Pre-Stress Current Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	381.59	67.52	412.38	711.01	4007.53	1028.05
N	Standard Error	147.36	59.16	217.26	432.16	3388.92	600.19
N	Median	56.13	8.87	9.92	9.97	568.86	19.61
N	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	#N/A
N	Standard Deviation	625.20	118.32	720.56	966.34	9585.32	4070.67
N	Variance	390880.60	14000.42	519203.56	933820.94	91878383.44	16570361.60
N	Kurtosis	1.62	4.00	0.83	-3.33	7.86	43.32
N	Skewness	1.69	2.00	1.50	0.61	2.80	6.50
N	Range	1983.44	237.65	1960.04	1783.88	27654.59	27658.44
N	Minimum	1.57	7.35	5.97	2.12	5.41	1.57
N	Maximum	1985.00	245.00	1966.00	1786.00	27660.00	27660.00
N	Sum	6868.67	270.08	4536.21	3555.03	32060.24	47290.23
N	Count	18.00	4.00	11.00	5.00	8.00	46.00
P	Mean	344.51	36.77	571.73	474.10	484.16	378.99
P	Standard Error	154.60	29.65	364.37	343.47	249.59	102.23
P	Median	34.51	8.17	11.02	10.63	17.92	12.27
P	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	#N/A
P	Standard Deviation	637.44	78.44	964.03	768.02	827.80	700.83
P	Variance	406332.84	6153.15	929350.45	589847.48	685254.42	491157.61
P	Kurtosis	4.17	6.96	-0.81	2.83	-0.07	1.32
P	Skewness	2.27	2.64	1.24	1.75	1.34	1.73
P	Range	2037.00	213.19	2040.35	1772.85	1972.94	2041.94
P	Minimum	1.00	1.31	1.65	3.15	0.07	0.07
P	Maximum	2038.00	214.50	2042.00	1776.00	1973.00	2042.00
P	Sum	5856.62	257.38	4002.12	2370.51	5325.77	17812.40
P	Count	17.00	7.00	7.00	5.00	11.00	47.00
ALL	Mean	363.58	47.95	474.35	592.55	1967.68	700.03
ALL	Standard Error	105.15	27.19	188.53	263.21	1438.30	301.56
ALL	Median	36.35	8.31	10.47	10.30	18.40	15.08
ALL	Mode	#N/A	#N/A	#N/A	#N/A	7.66	7.66
ALL	Standard Deviation	622.10	90.18	799.88	832.33	6269.41	2908.11
ALL	Variance	387009.42	8132.72	639809.39	692775.70	39305458.35	8457099.56
ALL	Kurtosis	2.24	2.21	-0.13	-1.38	18.33	82.61
ALL	Skewness	1.88	1.94	1.29	0.89	4.25	8.85
ALL	Range	2037.00	243.69	2040.35	1783.88	27659.94	27659.94
ALL	Minimum	1.00	1.31	1.65	2.12	0.07	0.07
ALL	Maximum	2038.00	245.00	2042.00	1786.00	27660.00	27660.00
ALL	Sum	12725.29	527.46	8538.34	5925.53	37386.01	65102.63
ALL	Count	35.00	11.00	18.00	10.00	19.00	93.00

Table 34. Censored Vendor A Pre-Stress Current Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	381.59	67.52	412.38	711.01	628.61	436.23
	Standard Error	147.36	59.16	217.26	432.16	300.37	102.11
	Median	56.13	8.87	9.92	9.97	33.72	16.79
	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	#N/A
	Standard Deviation	625.20	118.32	720.56	966.34	794.72	684.97
	Variance	390880.60	14000.42	519203.56	933820.94	631573.61	469183.57
	Kurtosis	1.62	4.00	0.83	-3.33	-1.71	-0.04
	Skewness	1.69	2.00	1.50	0.61	0.66	1.28
	Range	1983.44	237.65	1960.04	1783.88	1841.59	1983.44
	Minimum	1.57	7.35	5.97	2.12	5.41	1.57
	Maximum	1985.00	245.00	1966.00	1786.00	1847.00	1985.00
	Sum	6868.67	270.08	4536.21	3555.03	4400.24	19630.23
	Count	18.00	4.00	11.00	5.00	7.00	45.00
P	Mean	344.51	36.77	571.73	474.10	532.36	387.18
	Standard Error	154.60	29.65	364.37	343.47	270.74	104.14
	Median	34.51	8.17	11.02	10.63	18.16	12.76
	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	#N/A
	Standard Deviation	637.44	78.44	964.03	768.02	856.16	706.29
	Variance	406332.84	6153.15	929350.45	589847.48	733004.43	498848.95
	Kurtosis	4.17	6.96	-0.81	2.83	-0.56	1.19
	Skewness	2.27	2.64	1.24	1.75	1.19	1.70
	Range	2037.00	213.19	2040.35	1772.85	1972.94	2041.94
	Minimum	1.00	1.31	1.65	3.15	0.07	0.07
	Maximum	2038.00	214.50	2042.00	1776.00	1973.00	2042.00
	Sum	5856.62	257.38	4002.12	2370.51	5323.56	17810.19
	Count	17.00	7.00	7.00	5.00	10.00	46.00
ALL	Mean	363.58	47.95	474.35	592.55	571.99	411.43
	Standard Error	105.15	27.19	188.53	263.21	195.77	72.58
	Median	36.35	8.31	10.47	10.30	18.40	15.08
	Mode	#N/A	#N/A	#N/A	#N/A	7.66	7.66
	Standard Deviation	622.10	90.18	799.88	832.33	807.18	692.40
	Variance	387009.42	8132.72	639809.39	692775.70	651539.21	479411.17
	Kurtosis	2.24	2.21	-0.13	-1.38	-1.07	0.48
	Skewness	1.88	1.94	1.29	0.89	0.90	1.47
	Range	2037.00	243.69	2040.35	1783.88	1972.94	2041.94
	Minimum	1.00	1.31	1.65	2.12	0.07	0.07
	Maximum	2038.00	245.00	2042.00	1786.00	1973.00	2042.00
	Sum	12725.29	527.46	8538.34	5925.53	9723.80	37440.42
	Count	35.00	11.00	18.00	10.00	17.00	91.00

Table 35. Uncensored Vendor A Breakdown Voltage Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	25.78	26.55	26.59	26.58	23.98	25.81
	Standard Error	0.50	0.29	0.23	0.15	2.33	0.45
	Median	26.75	26.52	26.46	26.59	26.13	26.44
	Mode	26.89	#N/A	26.46	#N/A	26.32	26.89
	Standard Deviation	2.13	0.57	0.75	0.33	6.60	3.08
	Variance	4.55	0.33	0.56	0.11	43.50	9.50
	Kurtosis	-0.30	0.82	1.43	0.01	7.82	27.20
	Skewness	-1.04	0.25	-0.57	0.67	-2.78	-4.80
	Range	6.52	1.38	2.79	0.83	19.89	20.43
	Minimum	21.63	25.88	24.96	26.23	7.72	7.72
	Maximum	28.15	27.26	27.75	27.06	27.61	28.15
	Sum	464.02	106.18	292.49	132.89	191.83	1187.41
	Count	18.00	4.00	11.00	5.00	8.00	46.00
P	Mean	24.90	26.35	26.76	27.29	26.11	25.93
	Standard Error	0.55	0.21	0.17	0.56	0.36	0.25
	Median	25.86	26.18	26.89	26.74	26.04	26.29
	Mode	#N/A	#N/A	#N/A	#N/A	26.04	26.04
	Standard Deviation	2.28	0.55	0.45	1.25	1.18	1.75
	Variance	5.21	0.30	0.20	1.56	1.39	3.05
	Kurtosis	-1.32	5.21	-0.94	2.76	2.23	1.39
	Skewness	-0.34	2.21	-0.67	1.67	1.07	-1.08
	Range	7.34	1.57	1.18	3.10	4.29	8.41
	Minimum	20.99	25.97	26.04	26.30	24.57	20.99
	Maximum	28.33	27.54	27.22	29.40	28.86	29.40
	Sum	423.24	184.48	187.31	136.47	287.24	1218.74
	Count	17.00	7.00	7.00	5.00	11.00	47.00
ALL	Mean	25.35	26.42	26.66	26.94	25.21	25.87
	Standard Error	0.38	0.16	0.15	0.30	1.00	0.26
	Median	26.29	26.29	26.60	26.64	26.04	26.35
	Mode	26.89	26.41	26.46	26.59	26.04	26.04
	Standard Deviation	2.22	0.53	0.64	0.94	4.34	2.49
	Variance	4.92	0.29	0.41	0.88	18.86	6.18
	Kurtosis	-1.05	0.82	1.73	6.14	16.91	30.72
	Skewness	-0.64	1.28	-0.75	2.37	-4.00	-4.60
	Range	7.34	1.66	2.79	3.17	21.14	21.68
	Minimum	20.99	25.88	24.96	26.23	7.72	7.72
	Maximum	28.33	27.54	27.75	29.40	28.86	29.40
	Sum	887.26	290.66	479.80	269.36	479.07	2406.15
	Count	35.00	11.00	18.00	10.00	19.00	93.00

Table 36. Censored Vendor A Breakdown Voltage Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	25.78	26.55	26.59	26.58	26.30	26.22
N	Standard Error	0.50	0.29	0.23	0.15	0.24	0.22
N	Median	26.75	26.52	26.46	26.59	26.18	26.46
N	Mode	26.89	#N/A	26.46	#N/A	26.32	26.89
N	Standard Deviation	2.13	0.57	0.75	0.33	0.63	1.45
N	Variance	4.55	0.33	0.56	0.11	0.40	2.11
N	Kurtosis	-0.30	0.82	1.43	0.01	4.13	3.73
N	Skewness	-1.04	0.25	-0.57	0.67	1.69	-1.90
N	Range	6.52	1.38	2.79	0.83	2.04	6.52
N	Minimum	21.63	25.88	24.96	26.23	25.57	21.63
N	Maximum	28.15	27.26	27.75	27.06	27.61	28.15
N	Sum	464.02	106.18	292.49	132.89	184.11	1179.69
N	Count	18.00	4.00	11.00	5.00	7.00	45.00
P	Mean	24.90	26.35	26.76	27.29	25.84	25.87
P	Standard Error	0.55	0.21	0.17	0.56	0.25	0.25
P	Median	25.86	26.18	26.89	26.74	26.04	26.29
P	Mode	#N/A	#N/A	#N/A	#N/A	26.04	26.04
P	Standard Deviation	2.28	0.55	0.45	1.25	0.79	1.71
P	Variance	5.21	0.30	0.20	1.56	0.62	2.92
P	Kurtosis	-1.32	5.21	-0.94	2.76	-0.79	1.50
P	Skewness	-0.34	2.21	-0.67	1.67	-0.42	-1.18
P	Range	7.34	1.57	1.18	3.10	2.31	8.41
P	Minimum	20.99	25.97	26.04	26.30	24.57	20.99
P	Maximum	28.33	27.54	27.22	29.40	26.88	29.40
P	Sum	423.24	184.48	187.31	136.47	258.38	1189.88
P	Count	17.00	7.00	7.00	5.00	10.00	46.00
ALL	Mean	25.35	26.42	26.66	26.94	26.03	26.04
ALL	Standard Error	0.38	0.16	0.15	0.30	0.18	0.17
ALL	Median	26.29	26.29	26.60	26.64	26.04	26.35
ALL	Mode	26.89	26.41	26.46	26.59	26.04	26.04
ALL	Standard Deviation	2.22	0.53	0.64	0.94	0.74	1.59
ALL	Variance	4.92	0.29	0.41	0.88	0.55	2.52
ALL	Kurtosis	-1.05	0.82	1.73	6.14	0.78	2.15
ALL	Skewness	-0.64	1.28	-0.75	2.37	-0.15	-1.47
ALL	Range	7.34	1.66	2.79	3.17	3.04	8.41
ALL	Minimum	20.99	25.88	24.96	26.23	24.57	20.99
ALL	Maximum	28.33	27.54	27.75	29.40	27.61	29.40
ALL	Sum	887.26	290.66	479.80	269.36	442.49	2369.57
ALL	Count	35.00	11.00	18.00	10.00	17.00	91.00

Table 37. Uncensored Vendor A Breakdown Field Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	13.32	13.83	13.91	13.74	12.55	13.42
	Standard Error	0.26	0.14	0.13	0.14	1.23	0.24
	Median	13.85	13.75	14.00	13.60	14.00	13.90
	Mode	14.40	13.60	14.00	13.60	14.00	14.00
	Standard Deviation	1.12	0.29	0.44	0.31	3.48	1.62
	Variance	1.25	0.08	0.19	0.10	12.08	2.63
	Kurtosis	-1.40	-1.29	0.78	5.00	7.72	25.84
	Skewness	-0.67	0.85	-0.69	2.24	-2.76	-4.62
	Range	3.01	0.60	1.50	0.70	10.00	10.50
	Minimum	11.49	13.60	13.00	13.60	4.00	4.00
	Maximum	14.50	14.20	14.50	14.30	14.00	14.50
	Sum	239.80	55.30	153.00	68.70	100.40	617.20
	Count	18.00	4.00	11.00	5.00	8.00	46.00
P	Mean	12.99	13.73	13.93	14.16	14.36	13.69
	Standard Error	0.28	0.11	0.13	0.26	0.78	0.22
	Median	13.34	13.60	14.00	14.30	14.00	13.90
	Mode	11.62	13.60	14.00	14.30	14.00	14.00
	Standard Deviation	1.17	0.29	0.35	0.59	2.58	1.52
	Variance	1.36	0.09	0.12	0.34	6.65	2.30
	Kurtosis	-1.62	0.04	0.34	-0.61	9.97	19.78
	Skewness	-0.24	0.28	0.17	0.51	3.10	3.39
	Range	3.17	0.90	1.00	1.40	9.00	10.77
	Minimum	11.23	13.30	13.50	13.60	13.00	11.23
	Maximum	14.40	14.20	14.50	15.00	22.00	22.00
	Sum	220.85	96.10	97.50	70.80	158.00	643.25
	Count	17.00	7.00	7.00	5.00	11.00	47.00
ALL	Mean	13.16	13.76	13.92	13.95	13.60	13.55
	Standard Error	0.19	0.08	0.09	0.16	0.70	0.16
	Median	13.69	13.60	14.00	13.60	14.00	13.90
	Mode	14.40	13.60	14.00	13.60	14.00	14.00
	Standard Deviation	1.14	0.28	0.39	0.49	3.04	1.57
	Variance	1.30	0.08	0.15	0.25	9.24	2.45
	Kurtosis	-1.52	-0.50	0.52	0.57	8.67	23.06
	Skewness	-0.43	0.29	-0.50	1.18	-0.65	-0.97
	Range	3.27	0.90	1.50	1.40	18.00	18.00
	Minimum	11.23	13.30	13.00	13.60	4.00	4.00
	Maximum	14.50	14.20	14.50	15.00	22.00	22.00
	Sum	460.65	151.40	250.50	139.50	258.40	1260.45
	Count	35.00	11.00	18.00	10.00	19.00	93.00

Table 38. Censored Vendor A Breakdown Field Statistics.

	Statistics	0.10	0.30	0.50	0.70	1.00	Total
N	Mean	13.32	13.83	13.91	13.74	13.77	13.63
	Standard Error	0.26	0.14	0.13	0.14	0.15	0.12
	Median	13.85	13.75	14.00	13.60	14.00	13.90
	Mode	14.40	13.60	14.00	13.60	14.00	14.00
	Standard Deviation	1.12	0.29	0.44	0.31	0.41	0.79
	Variance	1.25	0.08	0.19	0.10	0.17	0.63
	Kurtosis	-1.40	-1.29	0.78	5.00	1.17	1.54
	Skewness	-0.67	0.85	-0.69	2.24	-1.56	-1.53
	Range	3.01	0.60	1.50	0.70	1.00	3.01
	Minimum	11.49	13.60	13.00	13.60	13.00	11.49
	Maximum	14.50	14.20	14.50	14.30	14.00	14.50
	Sum	239.80	55.30	153.00	68.70	96.40	613.20
	Count	18.00	4.00	11.00	5.00	7.00	45.00
P	Mean	12.99	13.73	13.93	14.16	13.60	13.51
	Standard Error	0.28	0.11	0.13	0.26	0.16	0.13
	Median	13.34	13.60	14.00	14.30	14.00	13.75
	Mode	11.62	13.60	14.00	14.30	14.00	14.00
	Standard Deviation	1.17	0.29	0.35	0.59	0.52	0.88
	Variance	1.36	0.09	0.12	0.34	0.27	0.78
	Kurtosis	-1.62	0.04	0.34	-0.61	-2.28	0.79
	Skewness	-0.24	0.28	0.17	0.51	-0.48	-1.17
	Range	3.17	0.90	1.00	1.40	1.00	3.77
	Minimum	11.23	13.30	13.50	13.60	13.00	11.23
	Maximum	14.40	14.20	14.50	15.00	14.00	15.00
	Sum	220.85	96.10	97.50	70.80	136.00	621.25
	Count	17.00	7.00	7.00	5.00	10.00	46.00
ALL	Mean	13.16	13.76	13.92	13.95	13.67	13.57
	Standard Error	0.19	0.08	0.09	0.16	0.11	0.09
	Median	13.69	13.60	14.00	13.60	14.00	13.90
	Mode	14.40	13.60	14.00	13.60	14.00	14.00
	Standard Deviation	1.14	0.28	0.39	0.49	0.47	0.84
	Variance	1.30	0.08	0.15	0.25	0.22	0.70
	Kurtosis	-1.52	-0.50	0.52	0.57	-1.50	1.00
	Skewness	-0.43	0.29	-0.50	1.18	-0.78	-1.32
	Range	3.27	0.90	1.50	1.40	1.00	3.77
	Minimum	11.23	13.30	13.00	13.60	13.00	11.23
	Maximum	14.50	14.20	14.50	15.00	14.00	15.00
	Sum	460.65	151.40	250.50	139.50	232.40	1234.45
	Count	35.00	11.00	18.00	10.00	17.00	91.00

Table 39. Uncensored Vendor B Capacitance Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
	Mean	24.33	24.65	24.62	24.54	24.67	24.74	24.56	24.65	24.61
	Standard Error	0.12	0.10	0.13	0.07	0.05	0.05	0.05	0.04	0.03
	Median	24.38	24.70	24.64	24.56	24.64	24.73	24.63	24.68	24.64
	Mode	#N/A	#N/A	#N/A	24.83	24.63	24.83	24.74	24.83	24.83
	Standard Deviation	0.44	0.19	0.43	0.31	0.25	0.26	0.38	0.29	0.33
	Variance	0.20	0.04	0.18	0.10	0.06	0.07	0.14	0.08	0.11
N	Kurtosis	-0.23	2.84	-1.17	-0.63	0.09	-0.79	0.88	-0.55	0.86
	Skewness	-0.62	-1.53	-0.35	0.18	0.49	-0.01	-0.73	-0.11	-0.62
	Range	1.50	0.44	1.21	1.16	0.98	0.90	1.84	1.16	1.84
	Minimum	23.41	24.37	23.93	24.06	24.27	24.27	23.41	24.06	23.41
	Maximum	24.91	24.81	25.14	25.22	25.25	25.17	25.25	25.22	25.25
	Sum	340.65	98.58	246.15	539.79	592.03	692.64	1178.83	1331.01	2509.84
	Count	14.00	4.00	10.00	22.00	24.00	28.00	48.00	54.00	102.00
	Mean	24.07	24.15	24.13	23.99	24.17	24.15	24.13	24.08	24.10
	Standard Error	0.07	0.09	0.10	0.06	0.04	0.06	0.04	0.04	0.03
	Median	24.21	24.16	24.14	23.93	24.16	24.20	24.16	24.09	24.14
	Mode	24.27	#N/A	24.13	24.08	#N/A	#N/A	24.27	24.08	24.27
	Standard Deviation	0.28	0.18	0.35	0.30	0.19	0.28	0.26	0.29	0.28
	Variance	0.08	0.03	0.13	0.09	0.04	0.08	0.07	0.08	0.08
P	Kurtosis	-0.80	-0.42	-0.48	-0.57	-0.55	-0.70	0.01	-0.76	-0.52
	Skewness	-0.68	-0.42	-0.42	0.18	0.20	-0.33	-0.52	-0.13	-0.31
	Range	0.94	0.42	1.14	1.16	0.69	1.00	1.14	1.16	1.17
	Minimum	23.52	23.92	23.49	23.46	23.86	23.58	23.49	23.46	23.46
	Maximum	24.46	24.34	24.63	24.62	24.55	24.58	24.63	24.62	24.63
	Sum	409.24	96.58	289.57	599.78	531.67	603.71	1230.48	1300.07	2530.55
	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
	Mean	24.19	24.40	24.35	24.25	24.43	24.46	24.34	24.36	24.35
	Standard Error	0.07	0.11	0.10	0.06	0.05	0.05	0.04	0.04	0.03
	Median	24.21	24.36	24.38	24.25	24.41	24.50	24.31	24.34	24.34
	Mode	24.27	#N/A	24.39	24.08	24.34	24.83	24.27	24.34	24.27
	Standard Deviation	0.38	0.32	0.45	0.41	0.34	0.40	0.39	0.41	0.40
A	Variance	0.14	0.10	0.20	0.17	0.11	0.16	0.15	0.17	0.16
L	Kurtosis	-0.37	-1.30	-0.54	-0.54	-0.39	-0.52	-0.22	-0.64	-0.48
L	Skewness	-0.10	-0.06	0.04	0.16	0.34	-0.21	0.02	-0.05	-0.02
	Range	1.50	0.89	1.65	1.76	1.39	1.59	1.84	1.76	1.84
	Minimum	23.41	23.92	23.49	23.46	23.86	23.58	23.41	23.46	23.41
	Maximum	24.91	24.81	25.14	25.22	25.25	25.17	25.25	25.22	25.25
	Sum	749.89	195.16	535.72	1139.57	1123.70	1296.35	2409.31	2631.08	5040.39
	Count	31.00	8.00	22.00	47.00	46.00	53.00	99.00	108.00	207.00
	Mean	24.23		24.28		24.44				
	Standard Error	0.06		0.05		0.04				
	Median	24.24		24.30		24.45				
	Mode	24.27		24.19		24.34				
	Standard Deviation	0.37		0.42		0.37				
C	Variance	0.14		0.18		0.14				
U	Kurtosis	-0.40		-0.57		-0.49				
M	Skewness	-0.17		0.14		0.00				
	Range	1.50		1.76		1.67				
	Minimum	23.41		23.46		23.58				
	Maximum	24.91		25.22		25.25				
	Sum	945.05		1675.29		2420.05				
	Count	39.00		69.00		99.00				

Table 40. Censored Vendor B Capacitance Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
N	Mean	24.43	24.65	24.68	24.54	24.67	24.74	24.61	24.65	24.63
	Standard Error	0.11	0.10	0.13	0.07	0.05	0.05	0.05	0.04	0.03
	Median	24.52	24.70	24.66	24.56	24.64	24.73	24.63	24.68	24.65
	Mode	#N/A	#N/A	#N/A	24.83	24.63	24.83	24.74	24.83	24.83
	Standard Deviation	0.37	0.19	0.40	0.31	0.25	0.26	0.33	0.29	0.31
	Variance	0.14	0.04	0.16	0.10	0.06	0.07	0.11	0.08	0.09
	Kurtosis	-0.65	2.84	-0.26	-0.63	0.09	-0.79	0.31	-0.55	-0.01
	Skewness	-0.53	-1.53	-0.66	0.18	0.49	-0.01	-0.45	-0.11	-0.32
	Range	1.19	0.44	1.21	1.16	0.98	0.90	1.53	1.16	1.53
	Minimum	23.72	24.37	23.93	24.06	24.27	24.27	23.72	24.06	23.72
	Maximum	24.91	24.81	25.14	25.22	25.25	25.17	25.25	25.22	25.25
	Sum	293.16	98.58	222.10	539.79	592.03	692.64	1107.29	1331.01	2438.30
	Count	12.00	4.00	9.00	22.00	24.00	28.00	45.00	54.00	99.00
P	Mean	24.07	24.15	24.13	23.99	24.17	24.15	24.13	24.08	24.10
	Standard Error	0.07	0.09	0.10	0.06	0.04	0.06	0.04	0.04	0.03
	Median	24.21	24.16	24.14	23.93	24.16	24.20	24.16	24.09	24.14
	Mode	24.27	#N/A	24.13	24.08	#N/A	#N/A	24.27	24.08	24.27
	Standard Deviation	0.28	0.18	0.35	0.30	0.19	0.28	0.26	0.29	0.28
	Variance	0.08	0.03	0.13	0.09	0.04	0.08	0.07	0.08	0.08
	Kurtosis	-0.80	-0.42	-0.48	-0.57	-0.55	-0.70	0.01	-0.76	-0.52
	Skewness	-0.68	-0.42	-0.42	0.18	0.20	-0.33	-0.52	-0.13	-0.31
	Range	0.94	0.42	1.14	1.16	0.69	1.00	1.14	1.16	1.17
	Minimum	23.52	23.92	23.49	23.46	23.86	23.58	23.49	23.46	23.46
	Maximum	24.46	24.34	24.63	24.62	24.55	24.58	24.63	24.62	24.63
	Sum	409.24	96.58	289.57	599.78	531.67	603.71	1230.48	1300.07	2530.55
	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
ALL	Mean	24.22	24.40	24.37	24.25	24.43	24.46	24.35	24.36	24.36
	Standard Error	0.07	0.11	0.10	0.06	0.05	0.05	0.04	0.04	0.03
	Median	24.24	24.36	24.39	24.25	24.41	24.50	24.33	24.34	24.34
	Mode	24.27	#N/A	24.39	24.08	24.34	24.83	24.27	24.34	24.27
	Standard Deviation	0.36	0.32	0.46	0.41	0.34	0.40	0.38	0.41	0.39
	Variance	0.13	0.10	0.21	0.17	0.11	0.16	0.14	0.17	0.16
	Kurtosis	-0.48	-1.30	-0.55	-0.54	-0.39	-0.52	-0.30	-0.64	-0.51
	Skewness	-0.01	-0.06	-0.05	0.16	0.34	-0.21	0.06	-0.05	0.00
	Range	1.39	0.89	1.65	1.76	1.39	1.59	1.76	1.76	1.79
	Minimum	23.52	23.92	23.49	23.46	23.86	23.58	23.49	23.46	23.46
	Maximum	24.91	24.81	25.14	25.22	25.25	25.17	25.25	25.22	25.25
	Sum	702.40	195.16	511.67	1139.57	1123.70	1296.35	2337.77	2631.08	4968.85
	Count	29.00	8.00	21.00	47.00	46.00	53.00	96.00	108.00	204.00
CUM	Mean	24.26		24.28		24.44				
	Standard Error	0.06		0.05		0.04				
	Median	24.27		24.30		24.45				
	Mode	24.27		24.19		24.34				
	Standard Deviation	0.36		0.42		0.37				
	Variance	0.13		0.18		0.14				
	Kurtosis	-0.56		-0.59		-0.49				
	Skewness	-0.08		0.12		0.00				
	Range	1.39		1.76		1.67				
	Minimum	23.52		23.46		23.58				
	Maximum	24.91		25.22		25.25				
	Sum	897.56		1651.24		2420.05				
	Count	37.00		68.00		99.00				

Table 41. Uncensored Vendor B Oxide Thickness Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
N	Mean	225.35	222.40	222.72	223.42	222.21	221.57	223.23	222.38	222.78
	Standard Error	1.10	0.87	1.23	0.61	0.45	0.44	0.50	0.36	0.30
	Median	224.85	221.90	222.45	223.20	222.45	221.60	222.55	222.15	222.40
	Mode	#N/A	#N/A	#N/A	220.70	220.70	220.70	220.00	220.70	220.70
	Standard Deviation	4.12	1.73	3.88	2.84	2.21	2.33	3.45	2.63	3.06
	Variance	16.95	3.01	15.04	8.08	4.90	5.41	11.89	6.93	9.35
	Kurtosis	-0.09	2.83	-1.13	-0.71	0.00	-0.80	1.13	-0.55	1.10
	Skewness	0.68	1.53	0.39	-0.14	-0.43	0.02	0.84	0.15	0.71
	Range	14.10	4.00	11.00	10.50	8.70	8.00	17.00	10.50	17.00
	Minimum	220.00	220.90	218.00	217.30	217.10	217.80	217.10	217.30	217.10
	Maximum	234.10	224.90	229.00	227.80	225.80	225.80	234.10	227.80	234.10
	Sum	3154.90	889.60	2227.20	4915.20	5333.10	6203.90	10715.20	12008.70	22723.90
	Count	14.00	4.00	10.00	22.00	24.00	28.00	48.00	54.00	102.00
P	Mean	227.81	227.00	227.15	228.66	226.81	227.08	227.22	227.80	227.52
	Standard Error	0.64	0.83	0.97	0.51	0.38	0.54	0.35	0.36	0.25
	Median	226.40	226.85	227.05	229.00	226.95	226.50	227.00	227.60	227.10
	Mode	225.80	#N/A	227.10	227.60	227.00	#N/A	226.40	227.60	226.40
	Standard Deviation	2.66	1.66	3.35	2.57	1.77	2.70	2.50	2.67	2.59
	Variance	7.07	2.77	11.20	6.62	3.12	7.31	6.23	7.10	6.70
	Kurtosis	-0.85	-0.34	-0.41	-0.87	-0.59	-0.79	0.03	-0.73	-0.49
	Skewness	0.60	0.46	0.48	0.15	-0.17	0.30	0.53	0.20	0.36
	Range	8.90	3.90	10.80	9.30	6.40	9.40	10.80	10.60	11.10
	Minimum	224.10	225.20	222.50	224.30	223.30	223.00	222.50	223.00	222.50
	Maximum	233.00	229.10	233.30	233.60	229.70	232.40	233.30	233.60	233.60
	Sum	3872.80	908.00	2725.80	5716.40	4989.80	5677.00	11588.40	12301.40	23889.80
	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
ALL	Mean	226.70	224.70	225.14	226.20	224.41	224.17	225.29	225.09	225.19
	Standard Error	0.64	1.03	0.89	0.55	0.45	0.51	0.36	0.36	0.26
	Median	226.40	225.05	224.85	226.60	224.55	223.70	225.50	225.20	225.30
	Mode	225.80	#N/A	224.70	226.60	223.30	220.70	225.80	220.70	220.70
	Standard Deviation	3.56	2.92	4.17	3.76	3.06	3.73	3.59	3.79	3.69
	Variance	12.67	8.52	17.41	14.12	9.35	13.90	12.90	14.36	13.61
	Kurtosis	-0.40	-1.28	-0.50	-0.47	-0.47	-0.54	-0.23	-0.64	-0.48
	Skewness	0.13	0.08	0.03	-0.15	-0.28	0.25	0.06	0.07	0.06
	Range	14.10	8.20	15.30	16.30	12.60	14.60	17.00	16.30	17.00
	Minimum	220.00	220.90	218.00	217.30	217.10	217.80	217.10	217.30	217.10
	Maximum	234.10	229.10	233.30	233.60	229.70	232.40	234.10	233.60	234.10
	Sum	7027.70	1797.60	4953.00	10631.60	10322.90	11880.90	22303.60	24310.10	46613.70
	Count	31.00	8.00	22.00	47.00	46.00	53.00	99.00	108.00	207.00
CUM	Mean	226.29		225.86		224.28				
	Standard Error	0.56		0.47		0.34				
	Median	226.10		226.00		224.20				
	Mode	225.80		226.60		220.70				
	Standard Deviation	3.50		3.90		3.42				
	Variance	12.24		15.18		11.69				
	Kurtosis	-0.41		-0.54		-0.50				
	Skewness	0.21		-0.12		0.06				
	Range	14.10		16.30		15.30				
	Minimum	220.00		217.30		217.10				
	Maximum	234.10		233.60		232.40				
	Sum	8825.30		15584.60		22203.80				
	Count	39.00		69.00		99.00				

Table 42. Censored Vendor B Oxide Thickness Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
	Mean	224.43	222.40	222.14	223.42	222.21	221.57	222.79	222.38	222.57
	Standard Error	0.99	0.87	1.21	0.61	0.45	0.44	0.44	0.36	0.28
	Median	223.55	221.90	222.30	223.20	222.45	221.60	222.50	222.15	222.40
	Mode	#N/A	#N/A	#N/A	220.70	220.70	220.70	220.00	220.70	220.70
	Standard Deviation	3.42	1.73	3.63	2.84	2.21	2.33	2.98	2.63	2.79
	Variance	11.70	3.01	13.19	8.08	4.90	5.41	8.89	6.93	7.78
N	Kurtosis	-0.53	2.83	-0.14	-0.71	0.00	-0.80	0.45	-0.55	0.08
	Skewness	0.58	1.53	0.70	-0.14	-0.43	0.02	0.54	0.15	0.38
	Range	11.10	4.00	11.00	10.50	8.70	8.00	14.00	10.50	14.00
	Minimum	220.00	220.90	218.00	217.30	217.10	217.80	217.10	217.30	217.10
	Maximum	231.10	224.90	229.00	227.80	225.80	225.80	231.10	227.80	231.10
	Sum	2693.20	889.60	1999.30	4915.20	5333.10	6203.90	10025.60	12008.70	22034.30
	Count	12.00	4.00	9.00	22.00	24.00	28.00	45.00	54.00	99.00
	Mean	227.81	227.00	227.15	228.66	226.81	227.08	227.22	227.80	227.52
	Standard Error	0.64	0.83	0.97	0.51	0.38	0.54	0.35	0.36	0.25
	Median	226.40	226.85	227.05	229.00	226.95	226.50	227.00	227.60	227.10
	Mode	225.80	#N/A	227.10	227.60	227.00	#N/A	226.40	227.60	226.40
	Standard Deviation	2.66	1.66	3.35	2.57	1.77	2.70	2.50	2.67	2.59
	Variance	7.07	2.77	11.20	6.62	3.12	7.31	6.23	7.10	6.70
P	Kurtosis	-0.85	-0.34	-0.41	-0.87	-0.59	-0.79	0.03	-0.73	-0.49
	Skewness	0.60	0.46	0.48	0.15	-0.17	0.30	0.53	0.20	0.36
	Range	8.90	3.90	10.80	9.30	6.40	9.40	10.80	10.60	11.10
	Minimum	224.10	225.20	222.50	224.30	223.30	223.00	222.50	223.00	222.50
	Maximum	233.00	229.10	233.30	233.60	229.70	232.40	233.30	233.60	233.60
	Sum	3872.80	908.00	2725.80	5716.40	4989.80	5677.00	11588.40	12301.40	23889.80
	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
	Mean	226.41	224.70	225.00	226.20	224.41	224.17	225.15	225.09	225.12
	Standard Error	0.63	1.03	0.92	0.55	0.45	0.51	0.36	0.36	0.26
	Median	226.10	225.05	224.70	226.60	224.55	223.70	225.35	225.20	225.20
	Mode	225.80	#N/A	224.70	226.60	223.30	220.70	225.80	220.70	220.70
	Standard Deviation	3.39	2.92	4.23	3.76	3.06	3.73	3.51	3.79	3.65
A	Variance	11.50	8.52	17.88	14.12	9.35	13.90	12.34	14.36	13.35
L	Kurtosis	-0.54	-1.28	-0.50	-0.47	-0.47	-0.54	-0.32	-0.64	-0.52
L	Skewness	0.03	0.08	0.12	-0.15	-0.28	0.25	0.01	0.07	0.05
	Range	13.00	8.20	15.30	16.30	12.60	14.60	16.20	16.30	16.50
	Minimum	220.00	220.90	218.00	217.30	217.10	217.80	217.10	217.30	217.10
	Maximum	233.00	229.10	233.30	233.60	229.70	232.40	233.30	233.60	233.60
	Sum	6566.00	1797.60	4725.10	10631.60	10322.90	11880.90	21614.00	24310.10	45924.10
	Count	29.00	8.00	21.00	47.00	46.00	53.00	96.00	108.00	204.00
	Mean	226.04		225.83		224.28				
	Standard Error	0.55		0.48		0.34				
	Median	225.90		225.80		224.20				
	Mode	225.80		226.60		220.70				
	Standard Deviation	3.33		3.92		3.42				
C	Variance	11.11		15.35		11.69				
U	Kurtosis	-0.59		-0.56		-0.50				
M	Skewness	0.11		-0.09		0.06				
	Range	13.00		16.30		15.30				
	Minimum	220.00		217.30		217.10				
	Maximum	233.00		233.60		232.40				
	Sum	8363.60		15356.70		22203.80				
	Count	37.00		68.00		99.00				

Table 43. Uncensored Vendor B Pre-Stress Current Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
N	Mean	6.72	9.42	5.38	7.13	5.75	9.13	5.96	8.34	7.22
	Standard Error	1.16	1.89	0.87	0.97	0.71	0.80	0.52	0.59	0.41
	Median	8.34	10.09	5.65	6.44	5.31	8.77	5.52	8.30	6.74
	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	#N/A	#N/A	12.95	4.54
	Standard Deviation	4.36	3.78	2.74	4.53	3.47	4.22	3.58	4.36	4.17
	Variance	18.97	14.29	7.48	20.56	12.04	17.77	12.84	19.04	17.39
	Kurtosis	-1.55	-1.17	0.55	-1.37	0.21	-0.44	-0.68	-0.99	-0.99
	Skewness	-0.12	-0.74	0.49	0.20	1.03	-0.23	0.56	-0.11	0.25
	Range	12.21	8.42	9.18	12.96	11.53	14.98	12.21	14.98	15.16
	Minimum	0.93	4.54	1.60	1.22	1.20	1.10	0.93	1.10	0.93
	Maximum	13.13	12.95	10.78	14.18	12.73	16.08	13.13	16.08	16.08
	Sum	94.13	37.67	53.78	156.78	138.07	255.67	285.97	450.11	736.08
	Count	14.00	4.00	10.00	22.00	24.00	28.00	48.00	54.00	102.00
P	Mean	5.92	12.57	5.75	6.27	6.12	8.60	5.96	7.82	6.92
	Standard Error	0.86	1.31	0.91	0.95	0.67	0.75	0.45	0.61	0.39
	Median	7.05	12.95	5.29	5.32	5.43	8.95	5.47	7.91	6.77
	Mode	8.01	#N/A	#N/A	#N/A	#N/A	#N/A	8.01	#N/A	8.01
	Standard Deviation	3.55	2.62	3.15	4.75	3.16	3.75	3.23	4.49	4.02
	Variance	12.63	6.84	9.95	22.59	10.01	14.09	10.46	20.13	16.15
	Kurtosis	-0.93	-1.45	0.10	-1.47	-0.09	-0.47	-0.54	-1.14	-0.97
	Skewness	-0.05	-0.62	0.76	0.21	0.65	-0.33	0.36	-0.21	0.15
	Range	12.18	5.87	10.20	13.35	11.05	14.23	12.18	15.01	15.01
	Minimum	0.35	9.26	2.03	0.35	1.43	0.11	0.35	0.11	0.11
	Maximum	12.53	15.12	12.23	13.70	12.47	14.34	12.53	15.12	15.12
	Sum	100.63	50.28	68.95	156.68	134.55	215.12	304.13	422.07	726.20
	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
ALL	Mean	6.28	10.99	5.58	6.67	5.93	8.88	5.96	8.08	7.06
	Standard Error	0.70	1.22	0.62	0.67	0.49	0.55	0.34	0.42	0.28
	Median	7.42	11.78	5.43	6.43	5.35	8.95	5.49	8.13	6.77
	Mode	8.01	#N/A	#N/A	#N/A	#N/A	#N/A	8.01	12.95	4.54
	Standard Deviation	3.89	3.45	2.91	4.62	3.30	3.97	3.39	4.41	4.09
	Variance	15.12	11.89	8.45	21.36	10.86	15.80	11.49	19.47	16.70
	Kurtosis	-1.22	0.42	0.05	-1.38	-0.09	-0.48	-0.63	-1.05	-0.97
	Skewness	-0.02	-0.85	0.65	0.18	0.83	-0.24	0.46	-0.16	0.20
	Range	12.78	10.59	10.63	13.83	11.53	15.97	12.78	15.97	15.97
	Minimum	0.35	4.54	1.60	0.35	1.20	0.11	0.35	0.11	0.11
	Maximum	13.13	15.12	12.23	14.18	12.73	16.08	13.13	16.08	16.08
	Sum	194.76	87.94	122.73	313.45	272.62	470.79	590.10	872.18	1462.28
	Count	31.00	8.00	22.00	47.00	46.00	53.00	99.00	108.00	207.00
CUM	Mean	7.25		6.32		7.51				
	Standard Error	0.68		0.50		0.40				
	Median	8.01		5.80		6.82				
	Mode	4.54		5.32		6.77				
	Standard Deviation	4.22		4.16		3.95				
	Variance	17.84		17.32		15.57				
	Kurtosis	-1.07		-1.05		-0.83				
	Skewness	-0.08		0.36		0.26				
	Range	14.77		13.83		15.97				
	Minimum	0.35		0.35		0.11				
	Maximum	15.12		14.18		16.08				
	Sum	282.70		436.18		743.40				
	Count	39.00		69.00		99.00				

Table 44. Censored Vendor B Pre-Stress Current Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
	Mean	6.45	9.42	5.36	7.13	5.75	9.13	5.86	8.34	7.21
	Standard Error	1.35	1.89	0.97	0.97	0.71	0.80	0.55	0.59	0.42
	Median	6.59	10.09	5.77	6.44	5.31	8.77	5.31	8.30	6.72
	Mode	#N/A	#N/A	#N/A	#N/A	#N/A	#N/A	#N/A	12.95	4.54
	Standard Deviation	4.68	3.78	2.90	4.53	3.47	4.22	3.67	4.36	4.23
	Variance	21.86	14.29	8.42	20.56	12.04	17.77	13.44	19.04	17.87
N	Kurtosis	-1.82	-1.17	0.20	-1.37	0.21	-0.44	-0.68	-0.99	-1.04
	Skewness	0.08	-0.74	0.50	0.20	1.03	-0.23	0.63	-0.11	0.25
	Range	12.21	8.42	9.18	12.96	11.53	14.98	12.21	14.98	15.16
	Minimum	0.93	4.54	1.60	1.22	1.20	1.10	0.93	1.10	0.93
	Maximum	13.13	12.95	10.78	14.18	12.73	16.08	13.13	16.08	16.08
	Sum	77.45	37.67	48.24	156.78	138.07	255.67	263.75	450.11	713.86
	Count	12.00	4.00	9.00	22.00	24.00	28.00	45.00	54.00	99.00
	Mean	5.92	12.57	5.75	6.27	6.12	8.60	5.96	7.82	6.92
	Standard Error	0.86	1.31	0.91	0.95	0.67	0.75	0.45	0.61	0.39
	Median	7.05	12.95	5.29	5.32	5.43	8.95	5.47	7.91	6.77
	Mode	8.01	#N/A	#N/A	#N/A	#N/A	#N/A	8.01	#N/A	8.01
	Standard Deviation	3.55	2.62	3.15	4.75	3.16	3.75	3.23	4.49	4.02
	Variance	12.63	6.84	9.95	22.59	10.01	14.09	10.46	20.13	16.15
P	Kurtosis	-0.93	-1.45	0.10	-1.47	-0.09	-0.47	-0.54	-1.14	-0.97
	Skewness	-0.05	-0.62	0.76	0.21	0.65	-0.33	0.36	-0.21	0.15
	Range	12.18	5.87	10.20	13.35	11.05	14.23	12.18	15.01	15.01
	Minimum	0.35	9.26	2.03	0.35	1.43	0.11	0.35	0.11	0.11
	Maximum	12.53	15.12	12.23	13.70	12.47	14.34	12.53	15.12	15.12
	Sum	100.63	50.28	68.95	156.68	134.55	215.12	304.13	422.07	726.20
	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
	Mean	6.14	10.99	5.58	6.67	5.93	8.88	5.92	8.08	7.06
	Standard Error	0.74	1.22	0.65	0.67	0.49	0.55	0.35	0.42	0.29
	Median	7.05	11.78	5.32	6.43	5.35	8.95	5.45	8.13	6.74
	Mode	8.01	#N/A	#N/A	#N/A	#N/A	#N/A	8.01	12.95	4.54
	Standard Deviation	3.98	3.45	2.98	4.62	3.30	3.97	3.43	4.41	4.11
A	Variance	15.88	11.89	8.87	21.36	10.86	15.80	11.73	19.47	16.92
L	Kurtosis	-1.28	0.42	-0.10	-1.38	-0.09	-0.48	-0.63	-1.05	-0.99
L	Skewness	0.08	-0.85	0.64	0.18	0.83	-0.24	0.50	-0.16	0.21
	Range	12.78	10.59	10.63	13.83	11.53	15.97	12.78	15.97	15.97
	Minimum	0.35	4.54	1.60	0.35	1.20	0.11	0.35	0.11	0.11
	Maximum	13.13	15.12	12.23	14.18	12.73	16.08	13.13	16.08	16.08
	Sum	178.08	87.94	117.19	313.45	272.62	470.79	567.88	872.18	1440.06
	Count	29.00	8.00	21.00	47.00	46.00	53.00	96.00	108.00	204.00
	Mean	7.19		6.33		7.51				
	Standard Error	0.71		0.51		0.40				
	Median	8.01		5.90		6.82				
	Mode	4.54		5.32		6.77				
	Standard Deviation	4.33		4.19		3.95				
C	Variance	18.76		17.57		15.57				
U	Kurtosis	-1.17		-1.08		-0.83				
M	Skewness	-0.03		0.35		0.26				
	Range	14.77		13.83		15.97				
	Minimum	0.35		0.35		0.11				
	Maximum	15.12		14.18		16.08				
	Sum	266.02		430.64		743.40				
	Count	37.00		68.00		99.00				

Table 45. Uncensored Vendor B Breakdown Voltage Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
N	Mean	30.30	29.92	31.09	29.40	28.89	28.16	29.76	28.79	29.25
	Standard Error	1.67	0.18	1.11	0.34	0.06	0.28	0.54	0.22	0.28
	Median	30.70	30.06	30.03	29.96	28.92	28.60	29.32	28.95	29.12
	Mode	40.98	#N/A	#N/A	#N/A	29.35	28.70	40.98	28.70	28.93
	Standard Deviation	6.26	0.37	3.52	1.57	0.29	1.46	3.76	1.59	2.85
	Variance	39.21	0.13	12.38	2.48	0.08	2.13	14.11	2.54	8.13
	Kurtosis	1.31	2.74	9.52	6.93	-0.01	10.91	6.49	6.14	10.81
	Skewness	-0.31	-1.68	3.06	-2.38	-0.43	-2.96	0.59	-2.03	0.79
	Range	22.67	0.79	11.59	6.93	1.13	7.29	22.71	8.69	22.71
	Minimum	18.31	29.38	29.43	23.83	28.22	22.07	18.31	22.07	18.31
	Maximum	40.98	30.17	41.02	30.76	29.35	29.36	41.02	30.76	41.02
	Sum	424.17	119.66	310.94	646.75	693.32	788.36	1428.43	1554.77	2983.20
	Count	14.00	4.00	10.00	22.00	24.00	28.00	48.00	54.00	102.00
P	Mean	28.15	29.11	30.01	29.44	29.50	29.33	29.17	29.36	29.27
	Standard Error	1.12	0.39	0.35	0.26	0.05	0.13	0.39	0.14	0.20
	Median	30.15	29.46	29.65	29.74	29.51	29.43	29.54	29.51	29.53
	Mode	#N/A	#N/A	29.52	29.59	29.29	#N/A	29.42	29.59	29.42
	Standard Deviation	4.63	0.77	1.21	1.29	0.22	0.66	2.79	1.00	2.06
	Variance	21.43	0.59	1.46	1.67	0.05	0.43	7.77	0.99	4.25
	Kurtosis	0.03	3.87	9.06	19.79	-0.52	6.23	7.33	22.27	14.04
	Skewness	-1.22	-1.96	2.87	-4.24	-0.07	-2.21	-2.58	-4.17	-3.35
	Range	14.80	1.61	4.61	6.82	0.83	3.08	14.80	6.82	14.80
	Minimum	19.20	27.96	29.04	23.55	29.03	27.02	19.20	23.55	19.20
	Maximum	34.00	29.57	33.65	30.37	29.86	30.10	34.00	30.37	34.00
	Sum	478.50	116.45	360.08	735.90	648.91	733.18	1487.49	1585.53	3073.02
	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
ALL	Mean	29.12	29.51	30.50	29.42	29.18	28.71	29.45	29.08	29.26
	Standard Error	0.98	0.25	0.54	0.21	0.06	0.18	0.33	0.13	0.17
	Median	30.52	29.54	29.79	29.79	29.26	29.02	29.51	29.38	29.43
	Mode	40.98	#N/A	29.52	29.59	29.28	28.70	29.51	29.59	29.42
	Standard Deviation	5.44	0.70	2.53	1.41	0.40	1.29	3.29	1.35	2.48
	Variance	29.61	0.50	6.38	2.00	0.16	1.65	10.82	1.83	6.13
	Kurtosis	0.96	3.74	15.78	10.47	-0.46	12.96	7.41	9.77	12.60
	Skewness	-0.38	-1.70	3.84	-3.05	-0.31	-3.00	-0.30	-2.69	-0.38
	Range	22.67	2.21	11.98	7.21	1.64	8.03	22.71	8.69	22.71
	Minimum	18.31	27.96	29.04	23.55	28.22	22.07	18.31	22.07	18.31
	Maximum	40.98	30.17	41.02	30.76	29.86	30.10	41.02	30.76	41.02
	Sum	902.67	236.11	671.02	1382.65	1342.23	1521.54	2915.92	3140.30	6056.22
	Count	31.00	8.00	22.00	47.00	46.00	53.00	99.00	108.00	207.00
CUM	Mean	29.20		29.76		28.93				
	Standard Error	0.78		0.23		0.10				
	Median	30.15		29.79		29.11				
	Mode	40.98		29.59		29.08				
	Standard Deviation	4.85		1.89		1.00				
	Variance	23.49		3.58		1.01				
	Kurtosis	1.93		20.76		22.14				
	Skewness	-0.48		2.25		-3.83				
	Range	22.67		17.47		8.03				
	Minimum	18.31		23.55		22.07				
	Maximum	40.98		41.02		30.10				
	Sum	1138.78		2053.67		2863.77				
	Count	39.00		69.00		99.00				

Table 46. Censored Vendor B Breakdown Voltage Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
	Mean	28.52	29.92	29.99	29.40	28.89	28.16	29.01	28.79	28.89
	Standard Error	1.36	0.18	0.16	0.34	0.06	0.28	0.36	0.22	0.20
	Median	30.56	30.06	30.01	29.96	28.92	28.60	29.16	28.95	29.08
	Mode	#N/A	#N/A	#N/A	#N/A	29.35	28.70	29.35	28.70	28.93
	Standard Deviation	4.71	0.37	0.49	1.57	0.29	1.46	2.43	1.59	2.01
	Variance	22.14	0.13	0.24	2.48	0.08	2.13	5.89	2.54	4.03
N	Kurtosis	2.49	2.74	-0.15	6.93	-0.01	10.91	15.11	6.14	14.54
	Skewness	-2.00	-1.68	0.70	-2.38	-0.43	-2.96	-3.74	-2.03	-3.37
	Range	13.04	0.79	1.49	6.93	1.13	7.29	13.04	8.69	13.04
	Minimum	18.31	29.38	29.43	23.83	28.22	22.07	18.31	22.07	18.31
	Maximum	31.35	30.17	30.92	30.76	29.35	29.36	31.35	30.76	31.35
	Sum	342.21	119.66	269.92	646.75	693.32	788.36	1305.45	1554.77	2860.22
	Count	12.00	4.00	9.00	22.00	24.00	28.00	45.00	54.00	99.00
	Mean	28.15	29.11	30.01	29.44	29.50	29.33	29.17	29.36	29.27
	Standard Error	1.12	0.39	0.35	0.26	0.05	0.13	0.39	0.14	0.20
	Median	30.15	29.46	29.65	29.74	29.51	29.43	29.54	29.51	29.53
	Mode	#N/A	#N/A	29.52	29.59	29.29	#N/A	29.42	29.59	29.42
	Standard Deviation	4.63	0.77	1.21	1.29	0.22	0.66	2.79	1.00	2.06
	Variance	21.43	0.59	1.46	1.67	0.05	0.43	7.77	0.99	4.25
P	Kurtosis	0.03	3.87	9.06	19.79	-0.52	6.23	7.33	22.27	14.04
	Skewness	-1.22	-1.96	2.87	-4.24	-0.07	-2.21	-2.58	-4.17	-3.35
	Range	14.80	1.61	4.61	6.82	0.83	3.08	14.80	6.82	14.80
	Minimum	19.20	27.96	29.04	23.55	29.03	27.02	19.20	23.55	19.20
	Maximum	34.00	29.57	33.65	30.37	29.86	30.10	34.00	30.37	34.00
	Sum	478.50	116.45	360.08	735.90	648.91	733.18	1487.49	1585.53	3073.02
	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
	Mean	28.30	29.51	30.00	29.42	29.18	28.71	29.09	29.08	29.08
	Standard Error	0.85	0.25	0.21	0.21	0.06	0.18	0.27	0.13	0.14
	Median	30.45	29.54	29.76	29.79	29.26	29.02	29.51	29.38	29.42
	Mode	30.67	#N/A	29.52	29.59	29.28	28.70	29.51	29.59	29.42
	Standard Deviation	4.58	0.70	0.95	1.41	0.40	1.29	2.61	1.35	2.04
A	Variance	20.98	0.50	0.90	2.00	0.16	1.65	6.83	1.83	4.16
L	Kurtosis	0.51	3.74	11.45	10.47	-0.46	12.96	9.56	9.77	13.62
L	Skewness	-1.44	-1.70	3.05	-3.05	-0.31	-3.00	-2.96	-2.69	-3.29
	Range	15.69	2.21	4.61	7.21	1.64	8.03	15.69	8.69	15.69
	Minimum	18.31	27.96	29.04	23.55	28.22	22.07	18.31	22.07	18.31
	Maximum	34.00	30.17	33.65	30.76	29.86	30.10	34.00	30.76	34.00
	Sum	820.71	236.11	630.00	1382.65	1342.23	1521.54	2792.94	3140.30	5933.24
	Count	29.00	8.00	21.00	47.00	46.00	53.00	96.00	108.00	204.00
	Mean	28.56		29.60		28.93				
	Standard Error	0.67		0.16		0.10				
	Median	30.14		29.79		29.11				
	Mode	30.67		29.59		29.08				
	Standard Deviation	4.08		1.31		1.00				
C	Variance	16.67		1.72		1.01				
U	Kurtosis	1.75		12.25		22.14				
M	Skewness	-1.75		-2.46		-3.83				
	Range	15.69		10.10		8.03				
	Minimum	18.31		23.55		22.07				
	Maximum	34.00		33.65		30.10				
	Sum	1056.82		2012.65		2863.77				
	Count	37.00		68.00		99.00				

Table 47. Uncensored Vendor B Breakdown Field Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
	Mean	13.44	13.40	13.95	13.16	13.00	12.71	13.32	12.95	13.12
	Standard Error	0.72	0.07	0.45	0.15	0.00	0.12	0.23	0.09	0.12
	Median	13.60	13.35	13.50	13.50	13.00	13.00	13.00	13.00	13.00
	Mode	13.60	13.30	13.50	13.50	13.00	13.00	13.00	13.00	13.00
	Standard Deviation	2.68	0.14	1.42	0.71	0.00	0.66	1.59	0.70	1.21
	Variance	7.21	0.02	2.02	0.51	0.00	0.43	2.52	0.49	1.47
N	Kurtosis	1.39	1.50	10.00	9.28	#DIV/0!	10.33	6.87	7.32	10.81
	Skewness	-0.57	1.41	3.16	-2.89	#DIV/0!	-2.97	0.05	-2.45	0.14
	Range	9.91	0.30	4.50	3.00	0.00	3.00	9.91	3.60	9.91
	Minimum	8.10	13.30	13.50	10.50	13.00	10.00	8.10	10.00	8.10
	Maximum	18.01	13.60	18.00	13.50	13.00	13.00	18.01	13.60	18.01
	Sum	188.09	53.60	139.50	289.50	312.00	356.00	639.59	699.10	1338.69
	Count	14.00	4.00	10.00	22.00	24.00	28.00	48.00	54.00	102.00
	Mean	12.42	12.83	13.21	12.88	13.00	12.92	12.85	12.89	12.87
	Standard Error	0.51	0.21	0.13	0.10	0.00	0.06	0.17	0.05	0.09
	Median	13.20	13.00	13.00	13.00	13.00	13.00	13.00	13.00	13.00
	Mode	13.60	13.00	13.00	13.00	13.00	13.00	13.00	13.00	13.00
	Standard Deviation	2.09	0.42	0.45	0.51	0.00	0.28	1.24	0.40	0.91
	Variance	4.37	0.18	0.20	0.26	0.00	0.08	1.55	0.16	0.83
P	Kurtosis	-0.16	3.77	6.77	22.84	#DIV/0!	9.64	7.00	24.78	13.83
	Skewness	-1.15	-1.92	2.54	-4.72	#DIV/0!	-3.30	-2.55	-4.69	-3.34
	Range	6.37	0.90	1.50	2.50	0.00	1.00	6.37	2.60	6.37
	Minimum	8.50	12.20	13.00	10.50	13.00	12.00	8.50	10.50	8.50
	Maximum	14.87	13.10	14.50	13.00	13.00	13.00	14.87	13.10	14.87
	Sum	211.06	51.30	158.50	322.00	286.00	323.00	655.56	696.30	1351.86
	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
	Mean	12.88	13.11	13.55	13.01	13.00	12.81	13.08	12.92	13.00
	Standard Error	0.43	0.15	0.23	0.09	0.00	0.07	0.14	0.05	0.07
	Median	13.50	13.20	13.50	13.00	13.00	13.00	13.00	13.00	13.00
	Mode	13.60	13.30	13.50	13.00	13.00	13.00	13.00	13.00	13.00
	Standard Deviation	2.39	0.42	1.06	0.62	0.00	0.52	1.43	0.57	1.07
A	Variance	5.72	0.18	1.12	0.39	0.00	0.27	2.05	0.32	1.15
L	Kurtosis	0.68	3.28	16.62	10.36	#DIV/0!	16.03	7.24	11.19	12.55
L	Skewness	-0.55	-1.54	3.90	-2.96	#DIV/0!	-3.63	-0.68	-2.95	-0.82
	Range	9.91	1.40	5.00	3.00	0.00	3.00	9.91	3.60	9.91
	Minimum	8.10	12.20	13.00	10.50	13.00	10.00	8.10	10.00	8.10
	Maximum	18.01	13.60	18.00	13.50	13.00	13.00	18.01	13.60	18.01
	Sum	399.15	104.90	298.00	611.50	598.00	679.00	1295.15	1395.40	2690.55
	Count	31.00	8.00	22.00	47.00	46.00	53.00	99.00	108.00	207.00
	Mean	12.92		13.18		12.90				
	Standard Error	0.34		0.10		0.04				
	Median	13.30		13.00		13.00				
	Mode	13.60		13.00		13.00				
	Standard Deviation	2.13		0.82		0.39				
C	Variance	4.56		0.67		0.15				
U	Kurtosis	1.59		20.14		31.78				
M	Skewness	-0.67		2.05		-5.11				
	Range	9.91		7.50		3.00				
	Minimum	8.10		10.50		10.00				
	Maximum	18.01		18.00		13.00				
	Sum	504.05		909.50		1277.00				
	Count	39.00		69.00		99.00				

Table 48. Censored Vendor B Breakdown Field Statistics.

	Statistics	.1 I	.1 II	.5 I	.5 II	1 I	1 II	I	II	Total
N	Mean	12.71	13.40	13.50	13.16	13.00	12.71	13.02	12.95	12.98
N	Standard Error	0.62	0.07	0.00	0.15	0.00	0.12	0.16	0.09	0.09
N	Median	13.60	13.35	13.50	13.50	13.00	13.00	13.00	13.00	13.00
N	Mode	13.60	13.30	13.50	13.50	13.00	13.00	13.00	13.00	13.00
N	Standard Deviation	2.13	0.14	0.00	0.71	0.00	0.66	1.10	0.70	0.90
N	Variance	4.54	0.02	0.00	0.51	0.00	0.43	1.21	0.49	0.81
N	Kurtosis	2.43	1.50	#DIV/0!	9.28	#DIV/0!	10.33	16.24	7.32	16.51
N	Skewness	-1.96	1.41	#DIV/0!	-2.89	#DIV/0!	-2.97	-3.94	-2.45	-3.71
N	Range	6.01	0.30	0.00	3.00	0.00	3.00	6.01	3.60	6.01
N	Minimum	8.10	13.30	13.50	10.50	13.00	10.00	8.10	10.00	8.10
N	Maximum	14.11	13.60	13.50	13.50	13.00	13.00	14.11	13.60	14.11
N	Sum	152.57	53.60	121.50	289.50	312.00	356.00	586.07	699.10	1285.17
N	Count	12.00	4.00	9.00	22.00	24.00	28.00	45.00	54.00	99.00
P	Mean	12.42	12.83	13.21	12.88	13.00	12.92	12.85	12.89	12.87
P	Standard Error	0.51	0.21	0.13	0.10	0.00	0.06	0.17	0.05	0.09
P	Median	13.20	13.00	13.00	13.00	13.00	13.00	13.00	13.00	13.00
P	Mode	13.60	13.00	13.00	13.00	13.00	13.00	13.00	13.00	13.00
P	Standard Deviation	2.09	0.42	0.45	0.51	0.00	0.28	1.24	0.40	0.91
P	Variance	4.37	0.18	0.20	0.26	0.00	0.08	1.55	0.16	0.83
P	Kurtosis	-0.16	3.77	6.77	22.84	#DIV/0!	9.64	7.00	24.78	13.83
P	Skewness	-1.15	-1.92	2.54	-4.72	#DIV/0!	-3.30	-2.55	-4.69	-3.34
P	Range	6.37	0.90	1.50	2.50	0.00	1.00	6.37	2.60	6.37
P	Minimum	8.50	12.20	13.00	10.50	13.00	12.00	8.50	10.50	8.50
P	Maximum	14.87	13.10	14.50	13.00	13.00	13.00	14.87	13.10	14.87
P	Sum	211.06	51.30	158.50	322.00	286.00	323.00	655.56	696.30	1351.86
P	Count	17.00	4.00	12.00	25.00	22.00	25.00	51.00	54.00	105.00
ALL	Mean	12.54	13.11	13.33	13.01	13.00	12.81	12.93	12.92	12.93
ALL	Standard Error	0.39	0.15	0.08	0.09	0.00	0.07	0.12	0.05	0.06
ALL	Median	13.30	13.20	13.50	13.00	13.00	13.00	13.00	13.00	13.00
ALL	Mode	13.60	13.30	13.50	13.00	13.00	13.00	13.00	13.00	13.00
ALL	Standard Deviation	2.07	0.42	0.37	0.62	0.00	0.52	1.18	0.57	0.90
ALL	Variance	4.30	0.18	0.13	0.39	0.00	0.27	1.38	0.32	0.82
ALL	Kurtosis	0.34	3.28	3.98	10.36	#DIV/0!	16.03	9.68	11.19	14.57
ALL	Skewness	-1.38	-1.54	1.48	-2.96	#DIV/0!	-3.63	-3.05	-2.95	-3.47
ALL	Range	6.77	1.40	1.50	3.00	0.00	3.00	6.77	3.60	6.77
ALL	Minimum	8.10	12.20	13.00	10.50	13.00	10.00	8.10	10.00	8.10
ALL	Maximum	14.87	13.60	14.50	13.50	13.00	13.00	14.87	13.60	14.87
ALL	Sum	363.63	104.90	280.00	611.50	598.00	679.00	1241.63	1395.40	2637.03
ALL	Count	29.00	8.00	21.00	47.00	46.00	53.00	96.00	108.00	204.00
CUM	Mean	12.66		13.11		12.90				
CUM	Standard Error	0.30		0.07		0.04				
CUM	Median	13.30		13.00		13.00				
CUM	Mode	13.60		13.00		13.00				
CUM	Standard Deviation	1.85		0.57		0.39				
CUM	Variance	3.44		0.33		0.15				
CUM	Kurtosis	1.50		11.95		31.78				
CUM	Skewness	-1.68		-2.73		-5.11				
CUM	Range	6.77		4.00		3.00				
CUM	Minimum	8.10		10.50		10.00				
CUM	Maximum	14.87		14.50		13.00				
CUM	Sum	468.53		891.50		1277.00				
CUM	Count	37.00		68.00		99.00				

APPENDIX E: DATA HISTOGRAMS

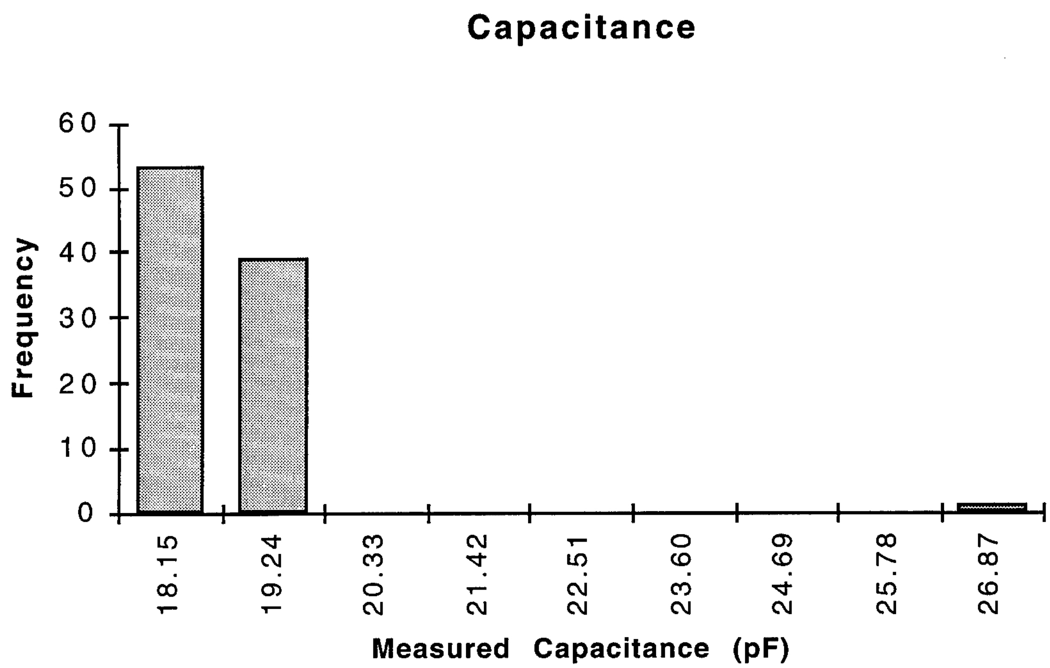

Figure 35. Uncensored Vendor A measured capacitance.

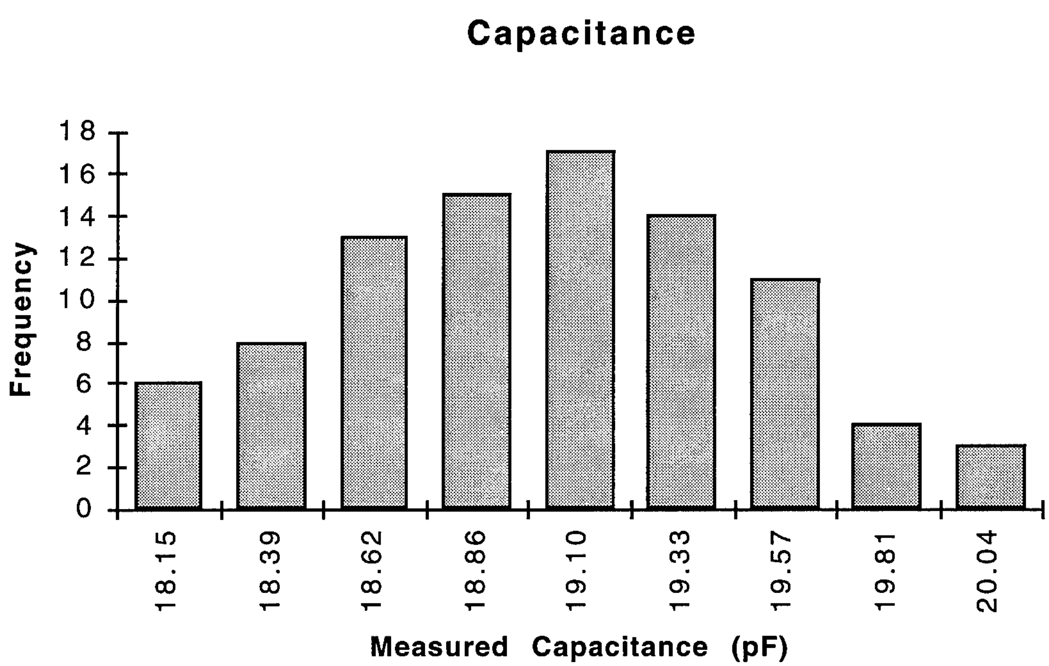

Figure 36. Censored Vendor A measured capacitance.

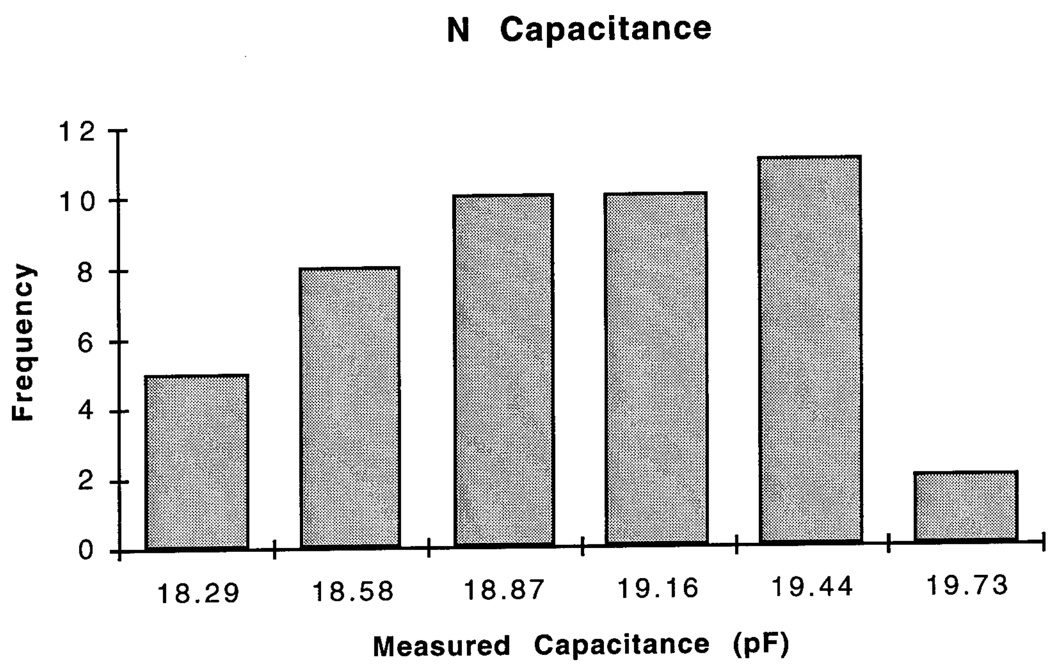

Figure 37. Uncensored Vendor A N structure measured capacitance.

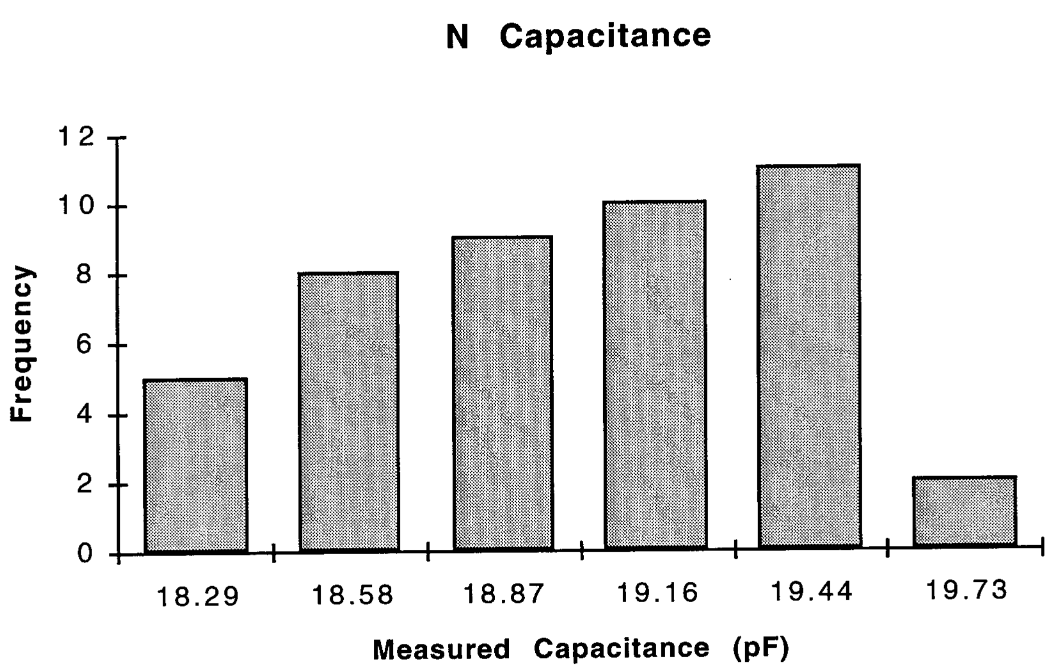

Figure 38. Censored Vendor A N structure measured capacitance.

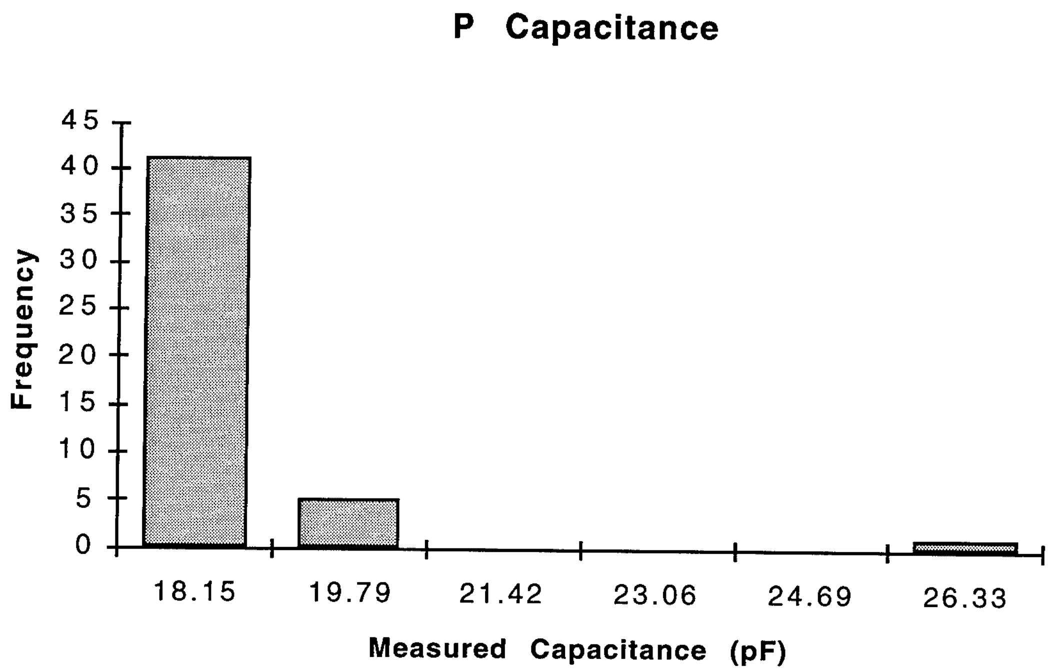

Figure 39. Uncensored Vendor A P structure measured capacitance.

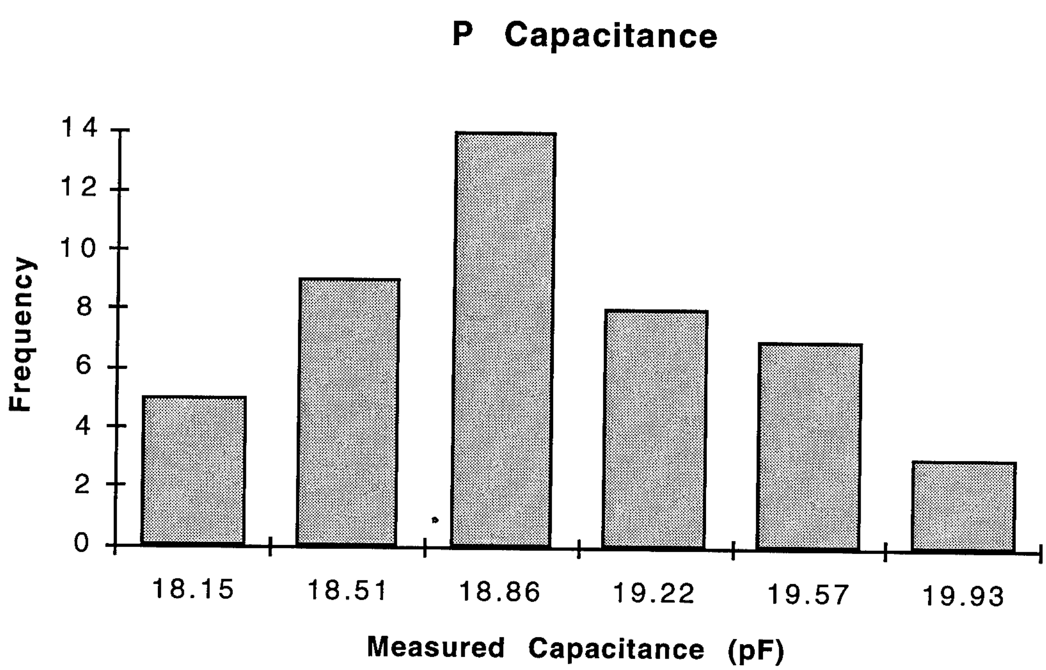

Figure 40. Censored Vendor A P structure measured capacitance.

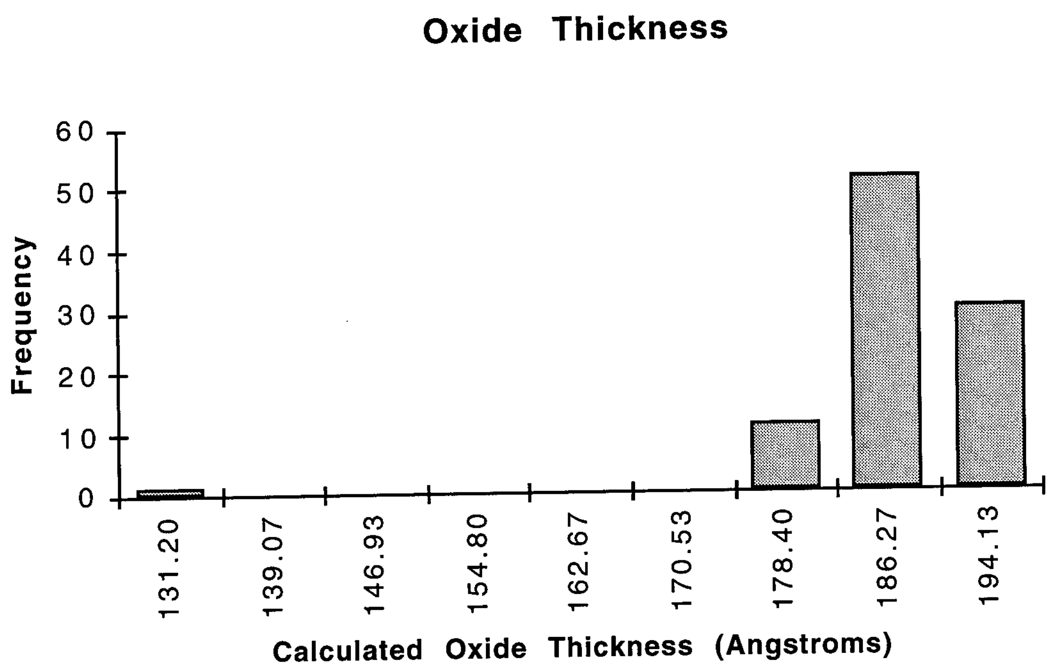

Figure 41. Uncensored Vendor A calculated oxide thickness.

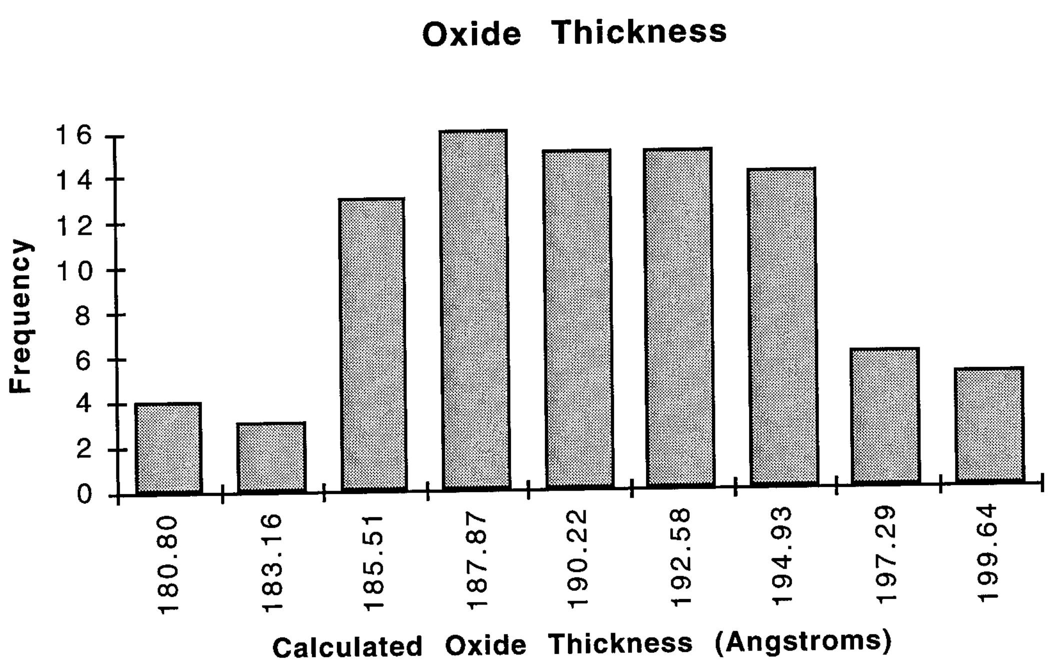

Figure 42. Censored Vendor A calculated oxide thickness.

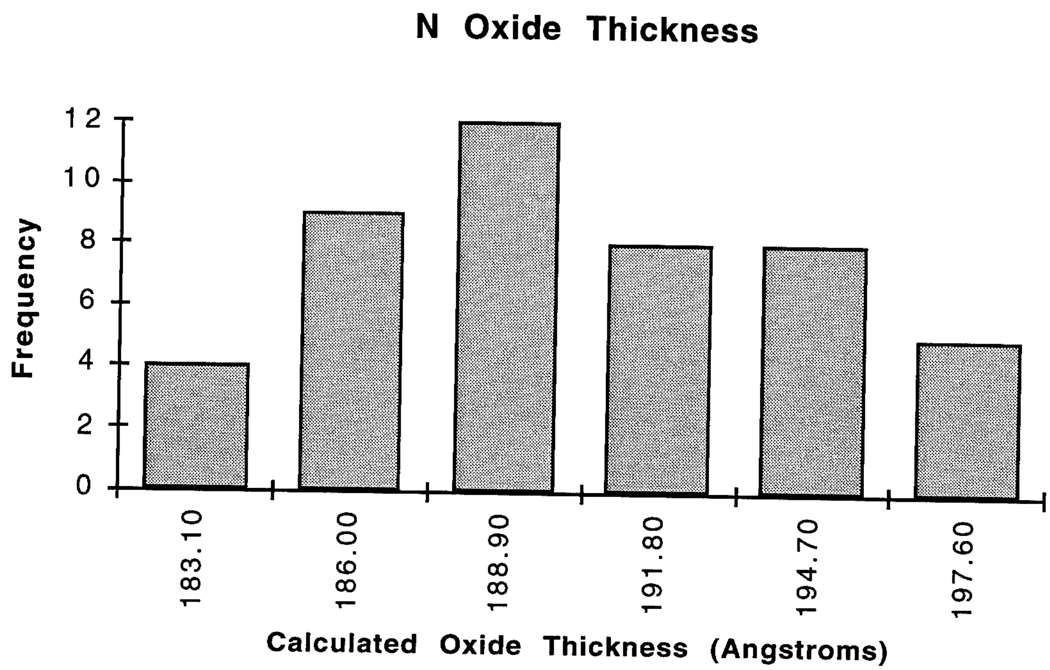

Figure 43. Uncensored Vendor A N structure calculated oxide thickness.

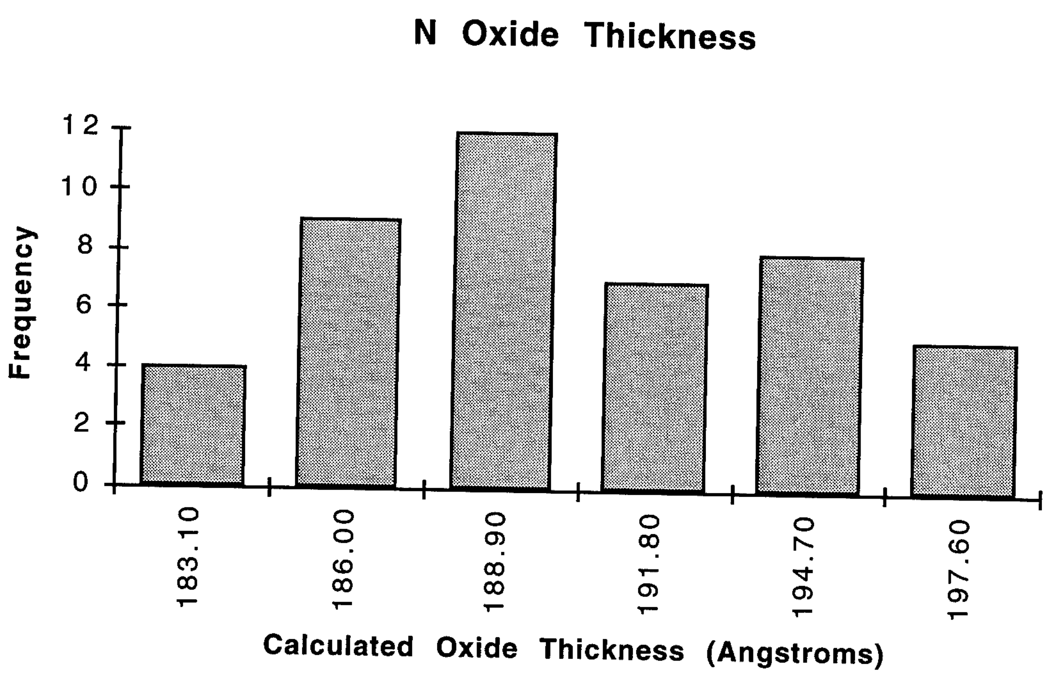

Figure 44. Censored Vendor A N structure calculated oxide thickness.

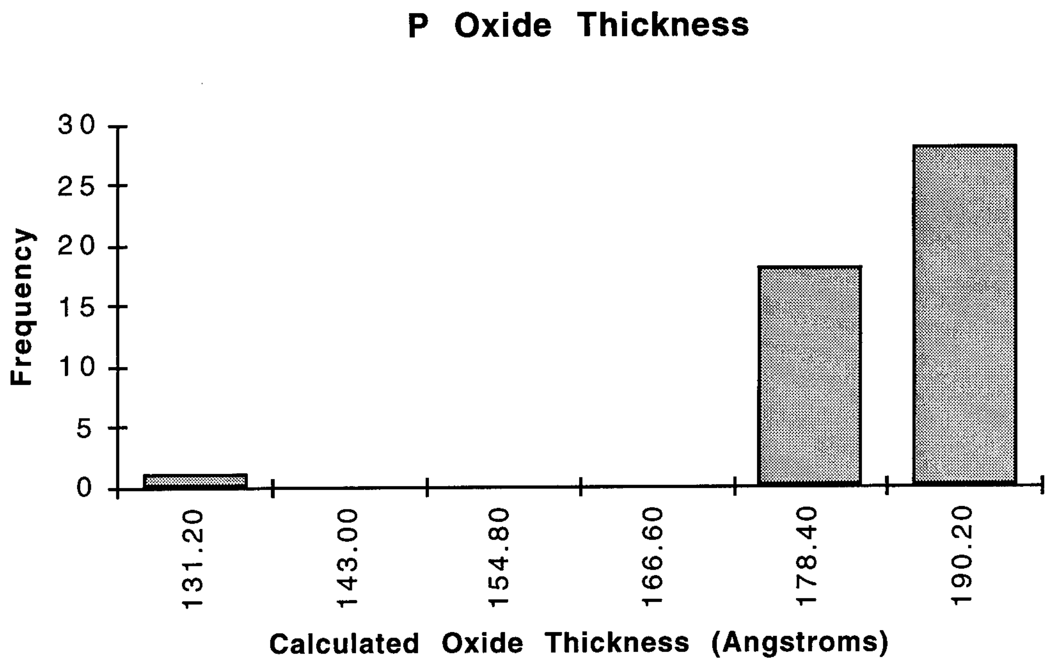

Figure 45. Uncensored Vendor A P structure calculated oxide thickness.

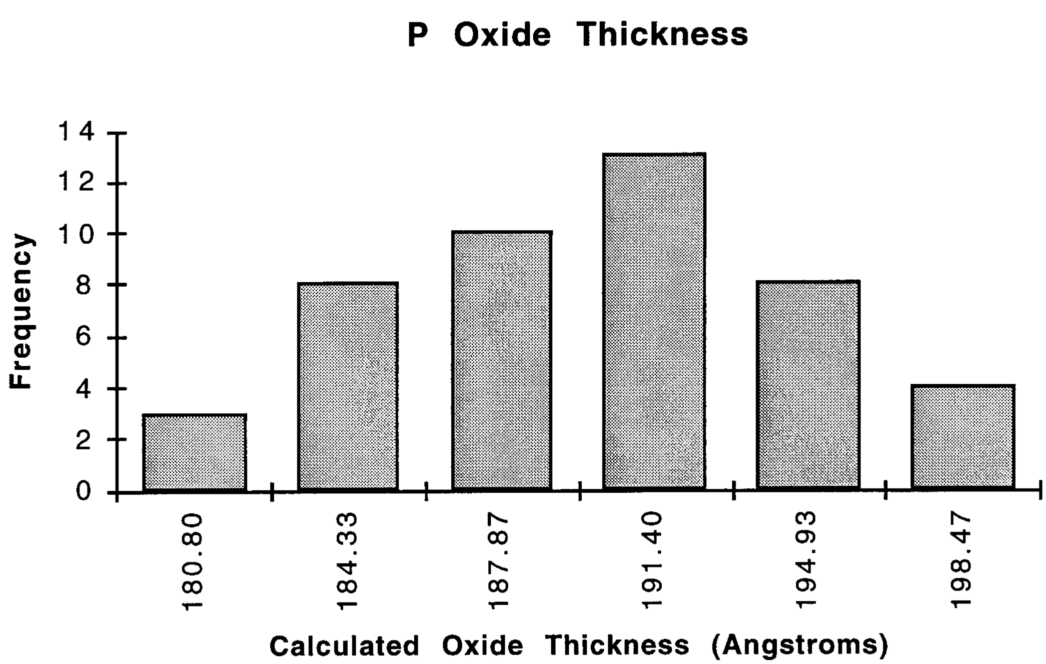

Figure 46. Censored Vendor A P structure calculated oxide thickness.

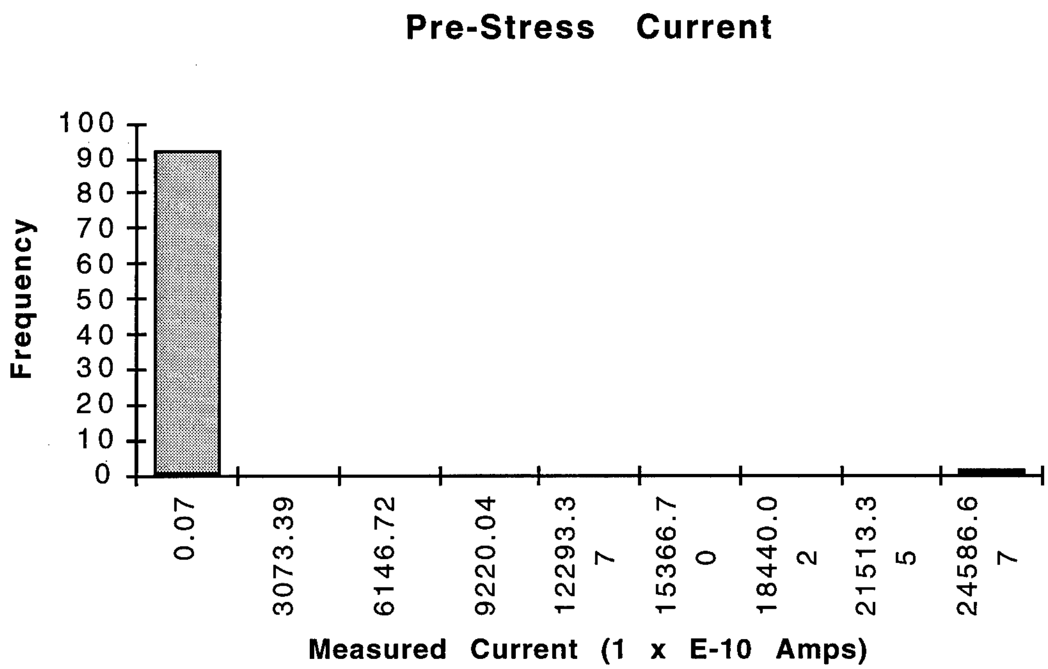

Figure 47. Uncensored Vendor A measured initial current.

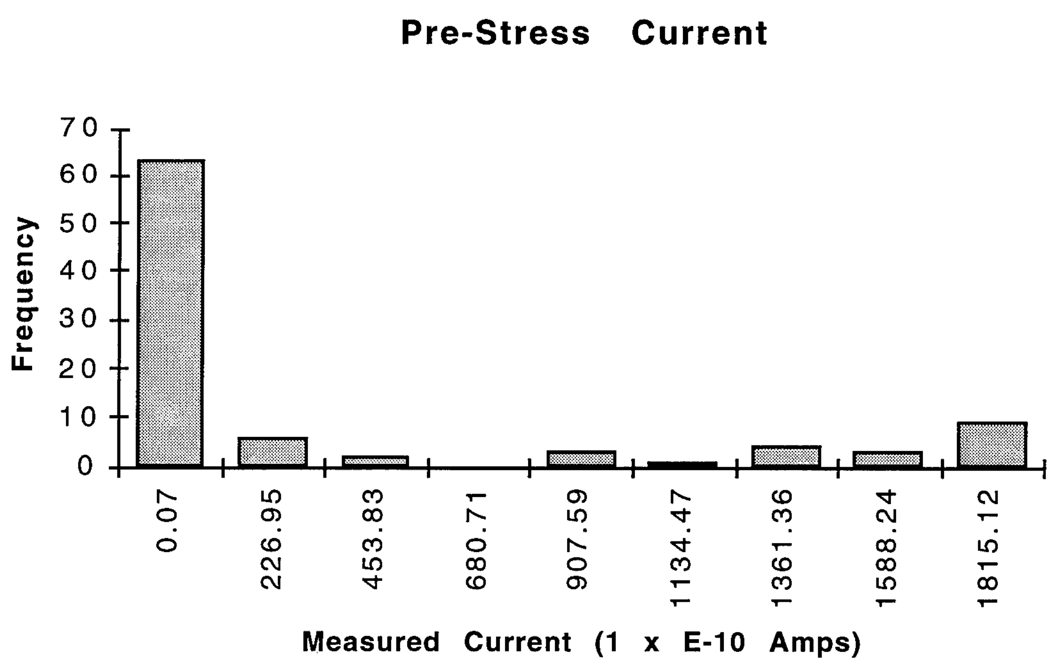

Figure 48. Censored Vendor A measured initial current.

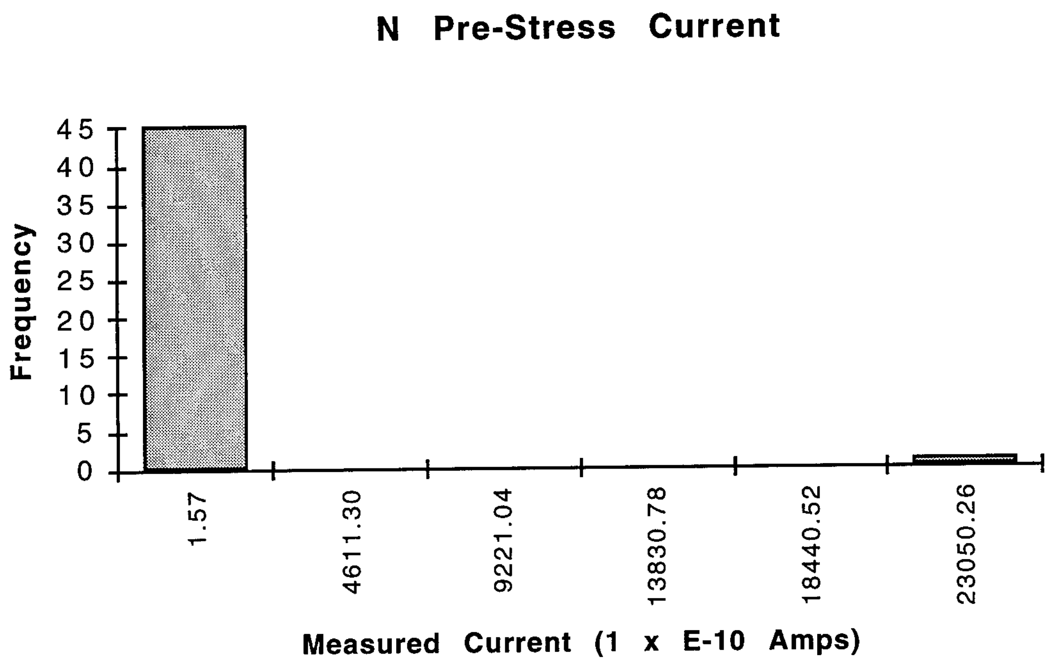

Figure 49. Uncensored Vendor A N structure measured initial current.

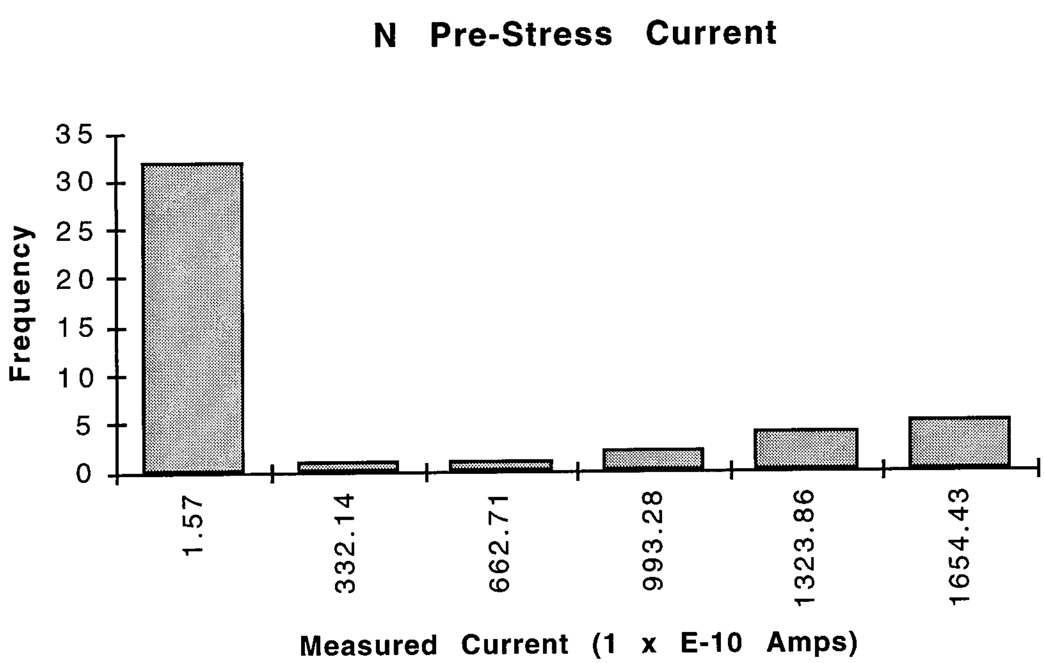

Figure 50. Censored Vendor A N structure measured initial current.

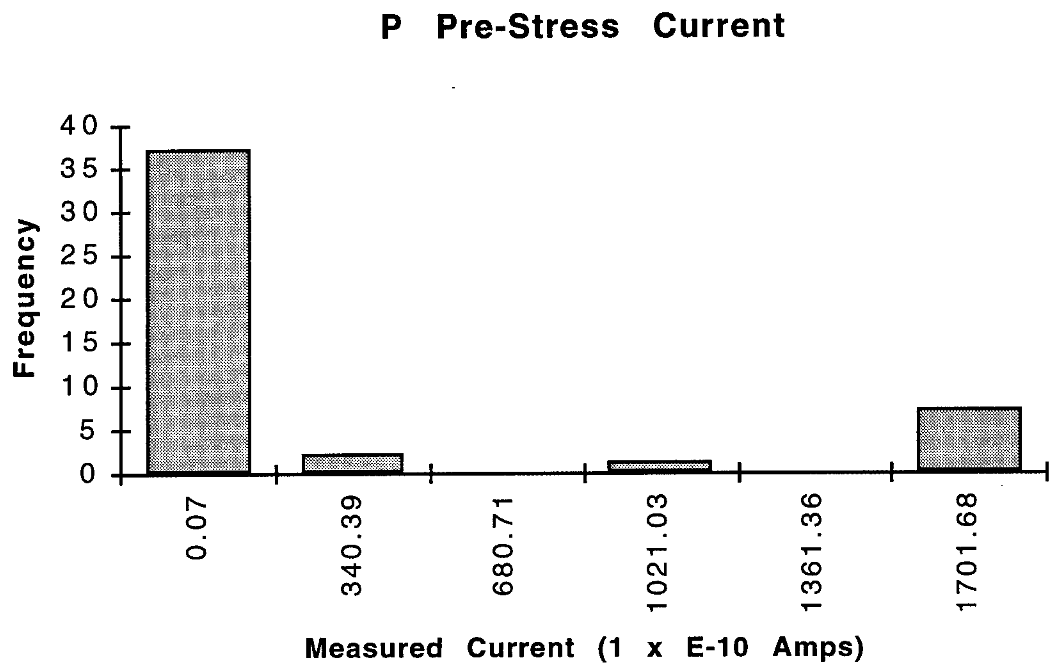

Figure 51. Uncensored Vendor A P structure measured initial current.

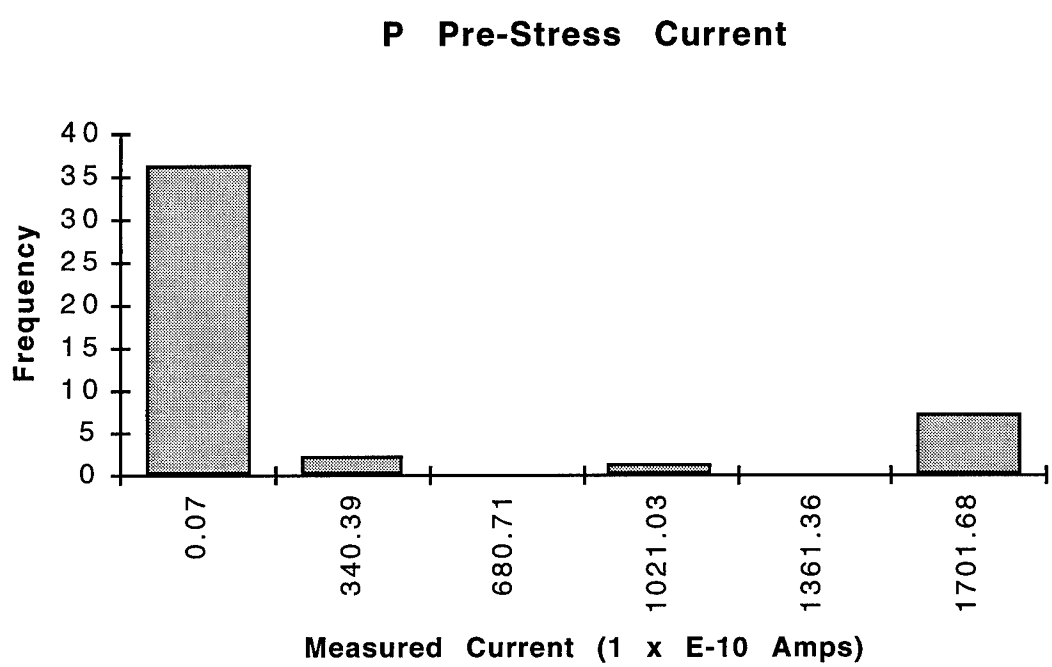

Figure 52. Censored Vendor A P structure measured initial current.

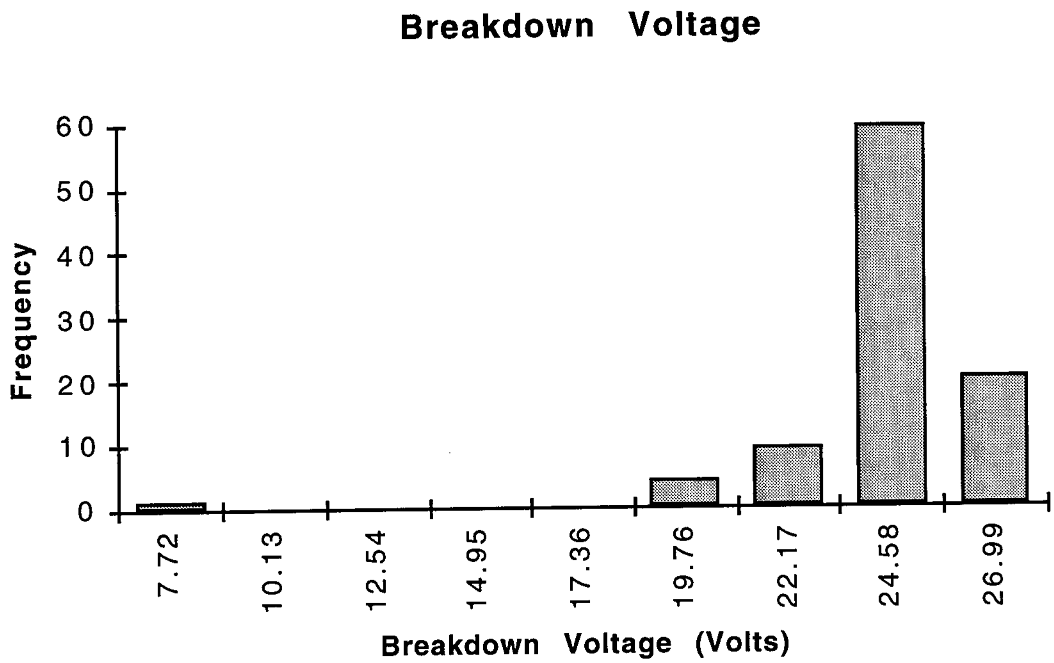

Figure 53. Uncensored Vendor A measured breakdown voltage.

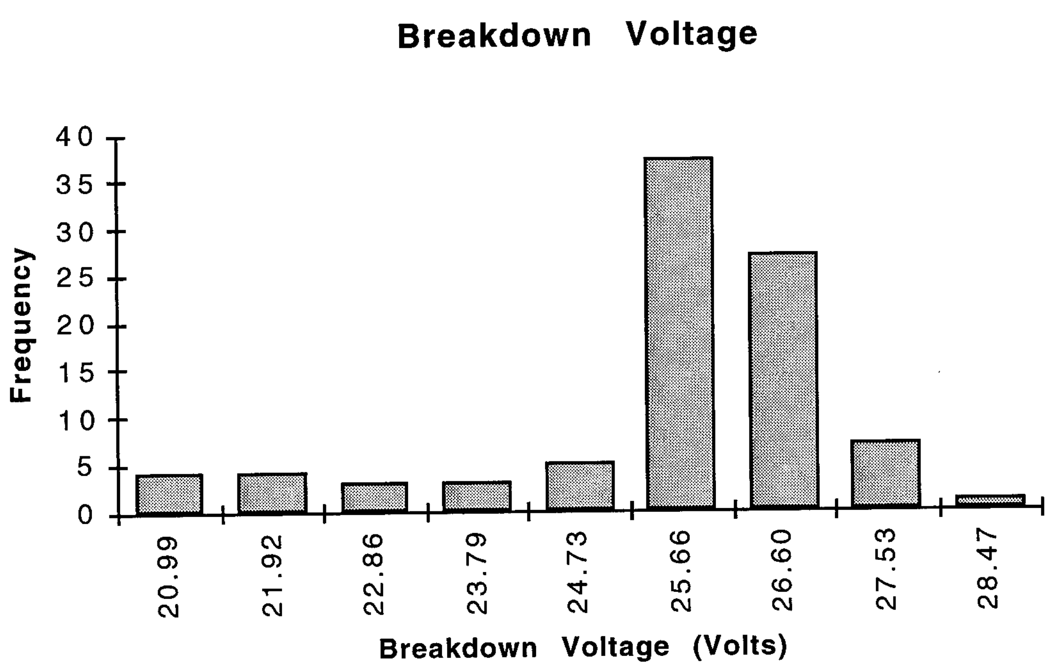

Figure 54. Censored Vendor A measured breakdown voltage.

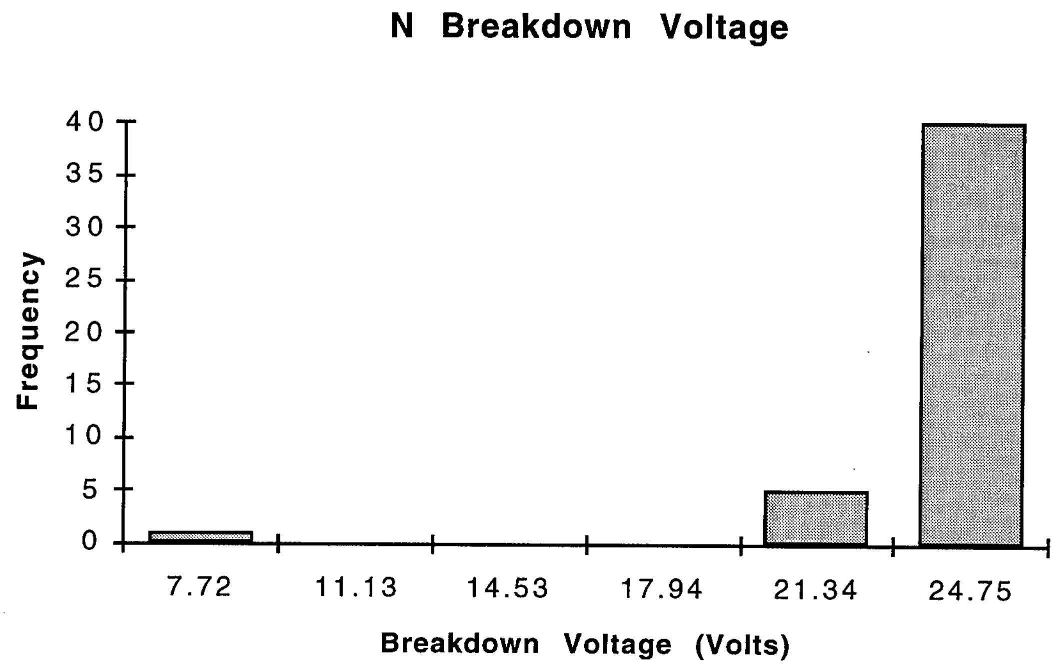

Figure 55. Uncensored Vendor A N structure measured breakdown voltage.

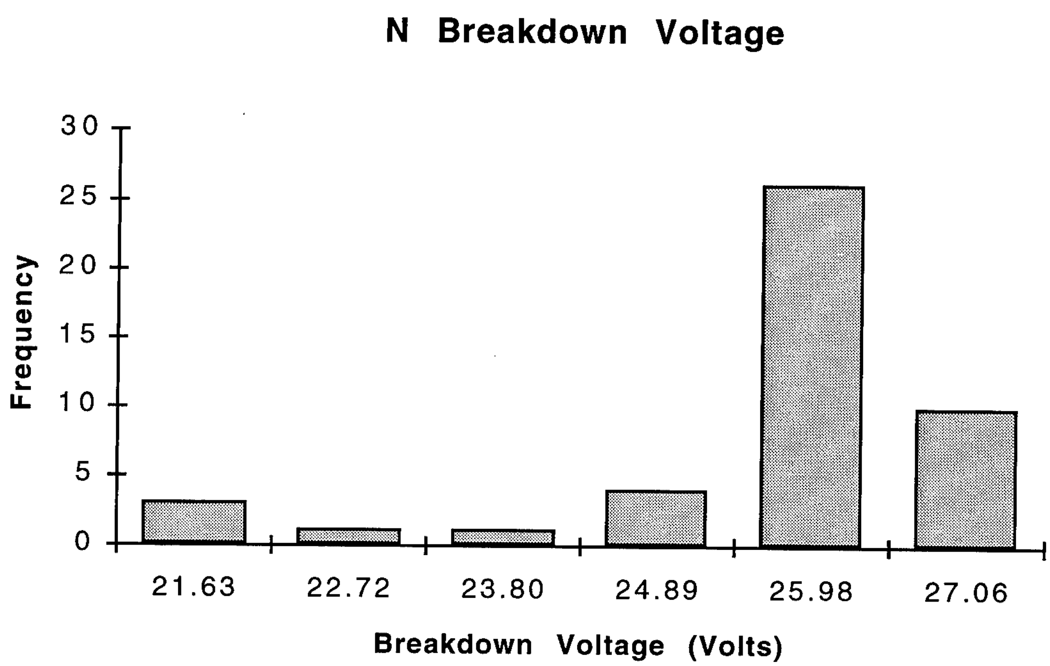

Figure 56. Censored Vendor A N structure measured breakdown voltage.

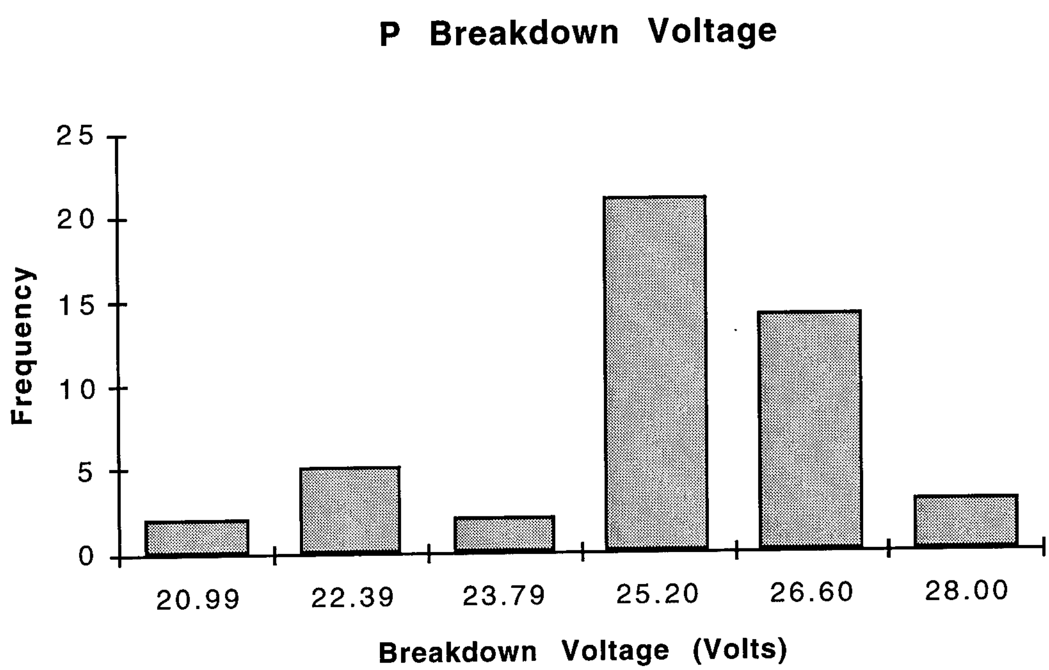

Figure 57. Uncensored Vendor A P structure measured breakdown voltage.

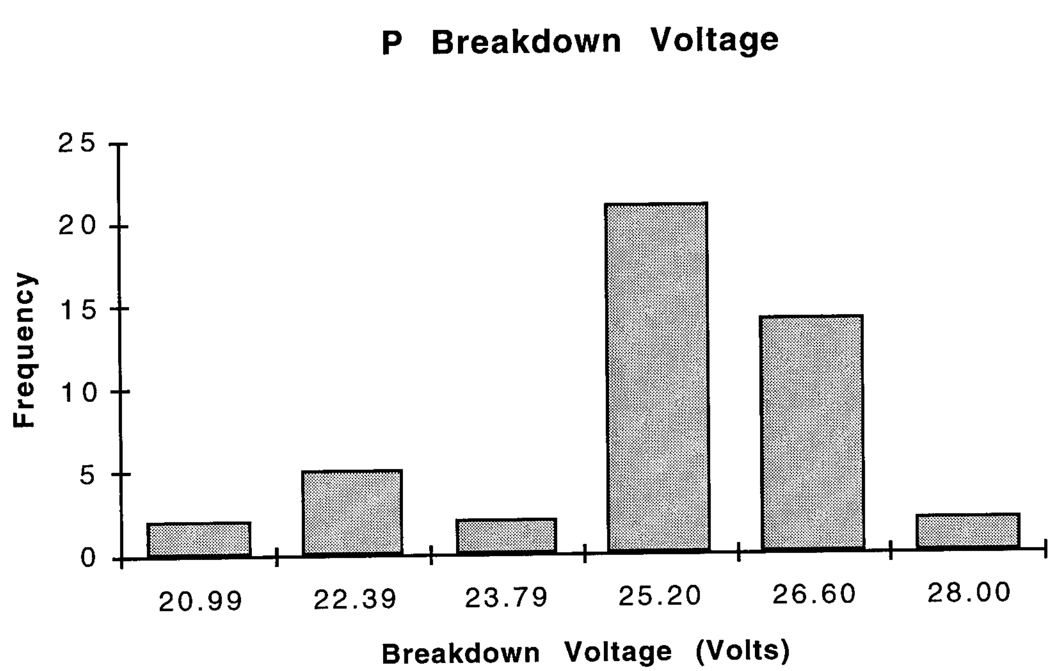

Figure 58. Censored Vendor A P structure measured breakdown voltage.

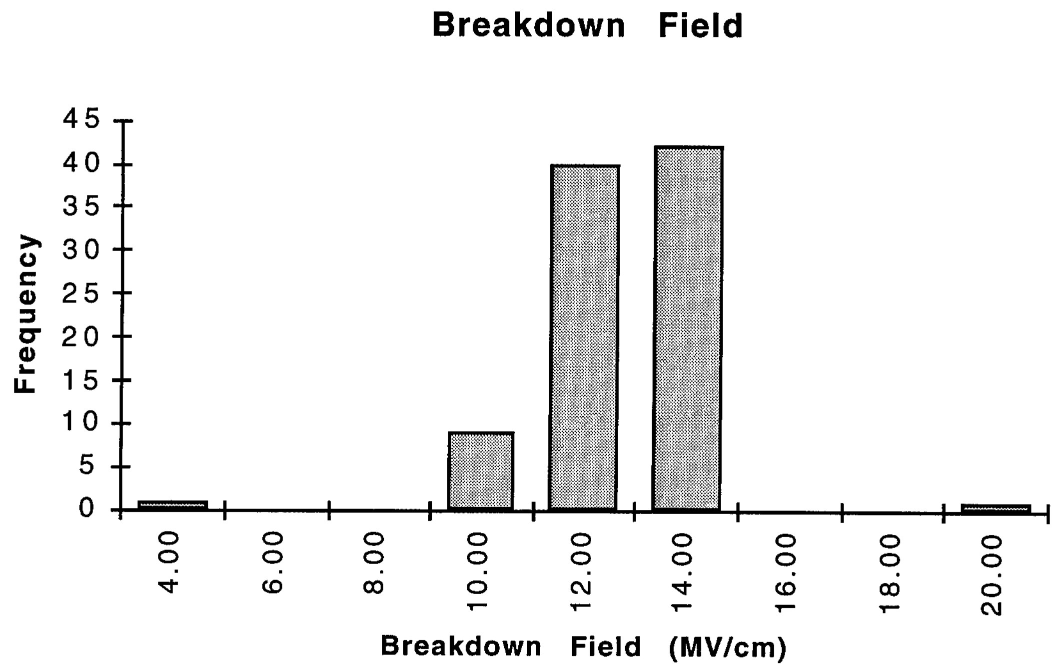

Figure 59. Uncensored Vendor A calculated breakdown field.

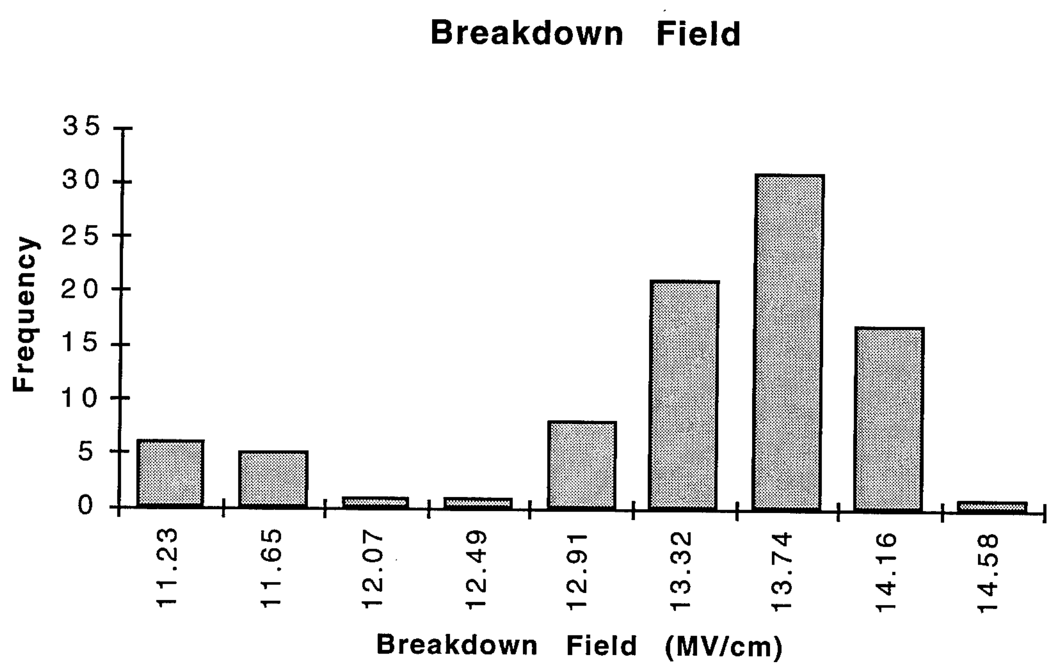

Figure 60. Censored Vendor A calculated breakdown field.

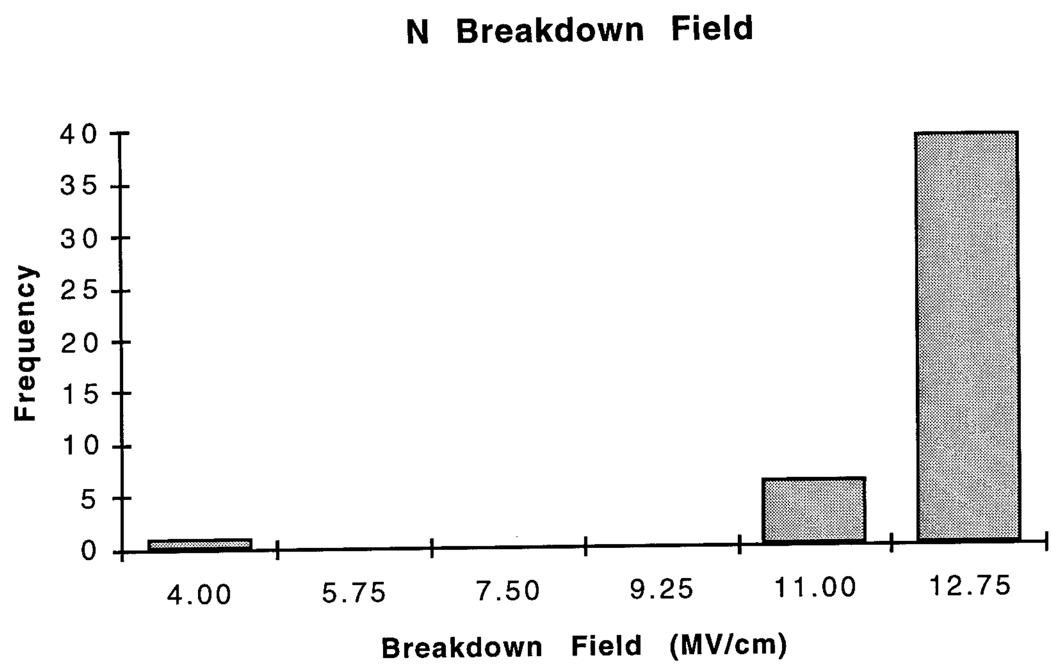

Figure 61. Uncensored Vendor A N structure calculated breakdown field.

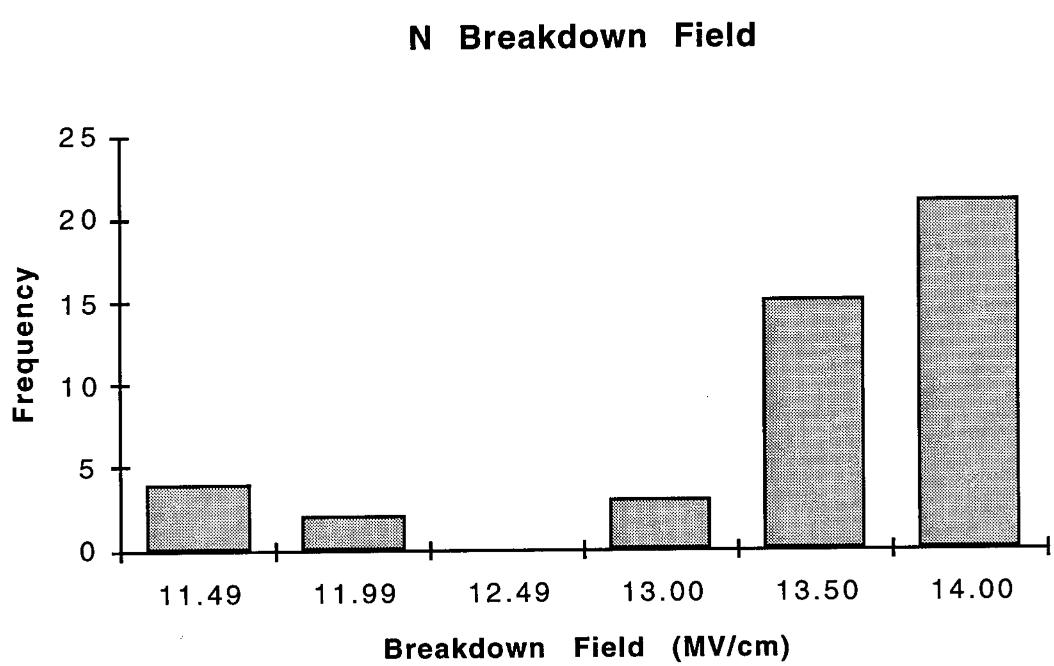

Figure 62. Censored Vendor A N structure calculated breakdown field.

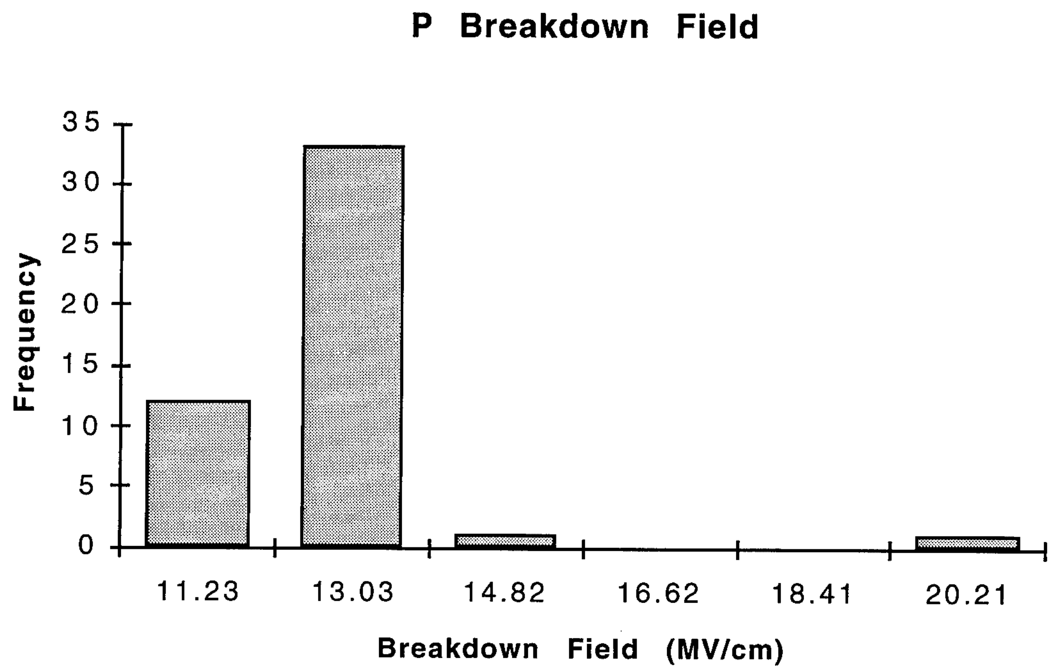

Figure 63. Uncensored Vendor A P structure calculated breakdown field.

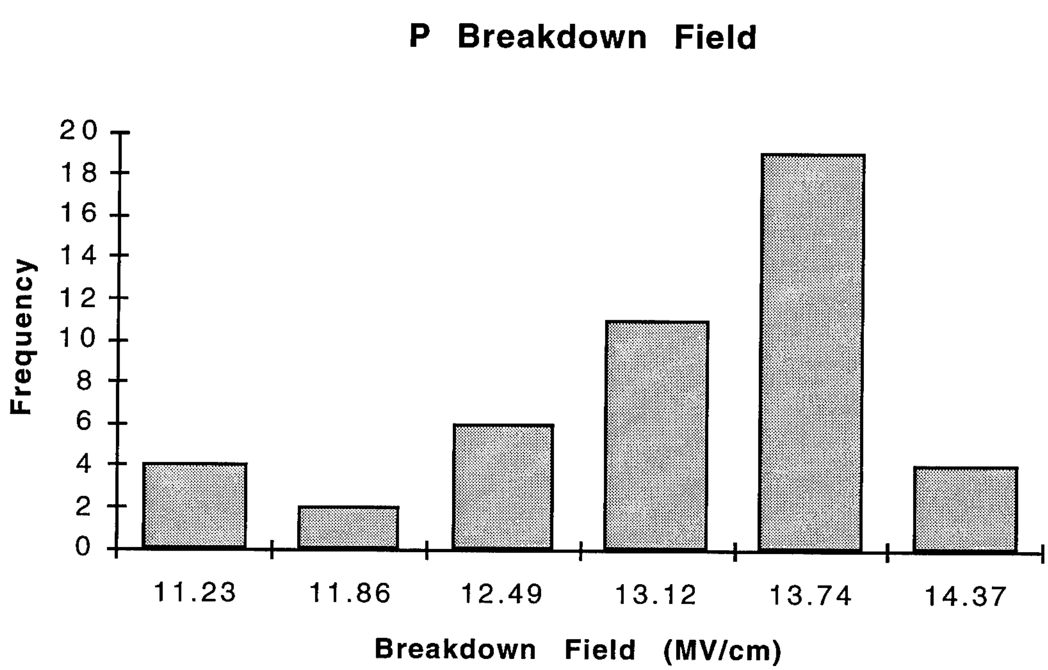

Figure 64. Censored Vendor A P structure calculated breakdown field.

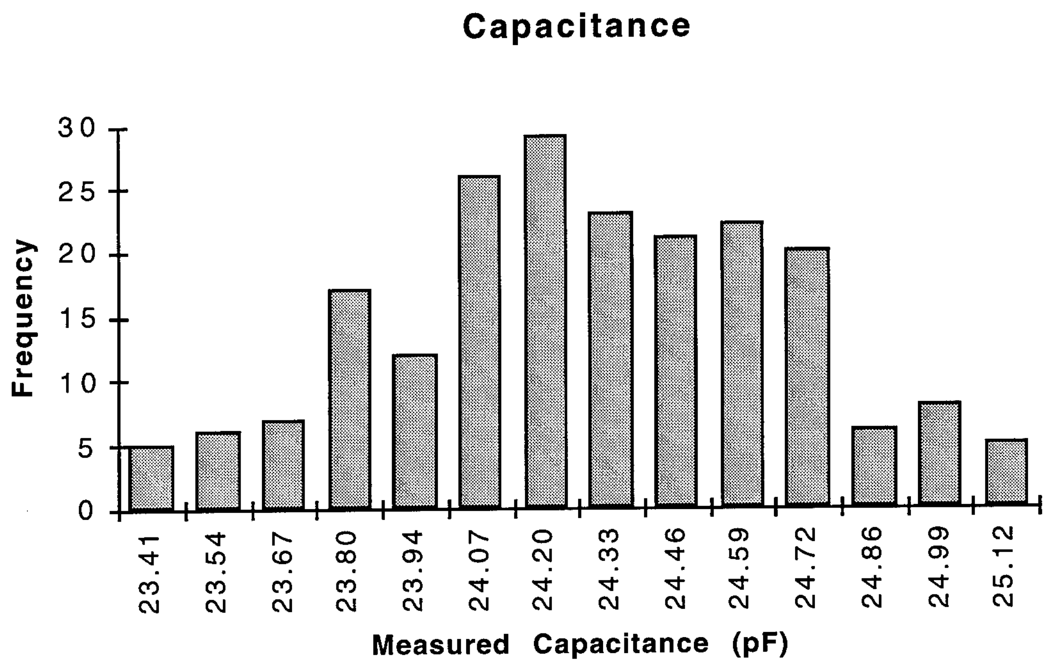

Figure 65. Uncensored Vendor B measured capacitance.

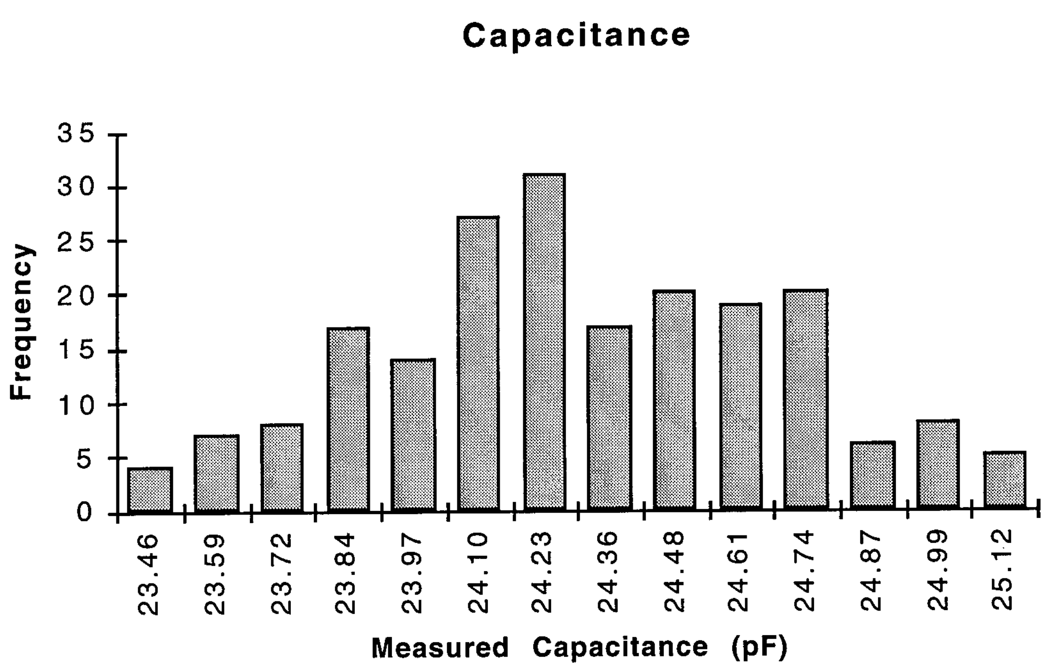

Figure 66. Censored Vendor B measured capacitance.

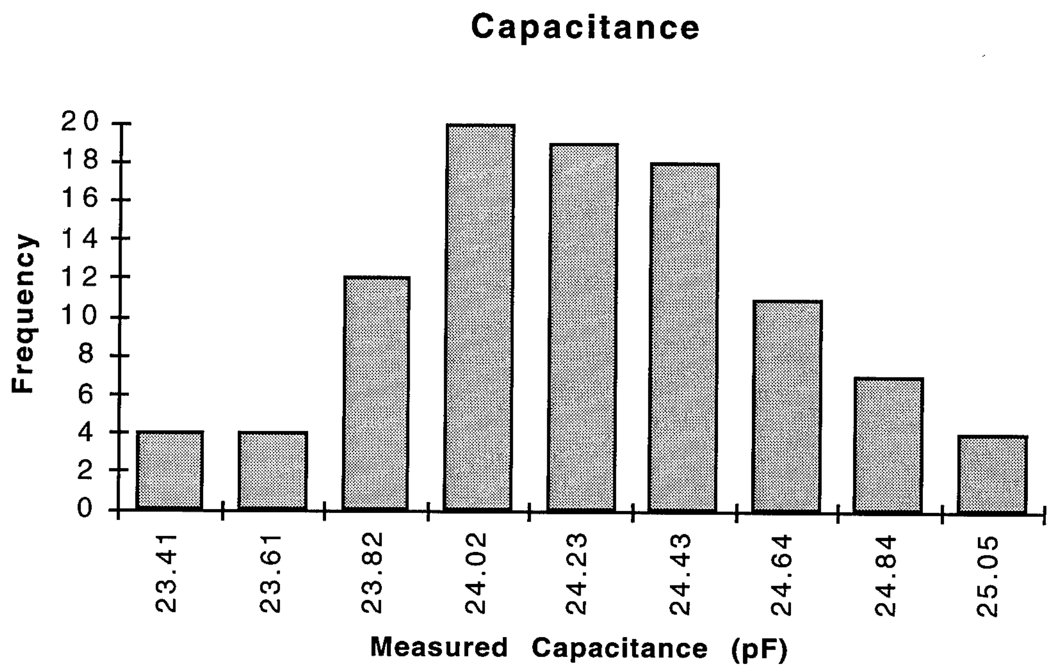

Figure 67. Uncensored Vendor B Wafer 1 measured capacitance.

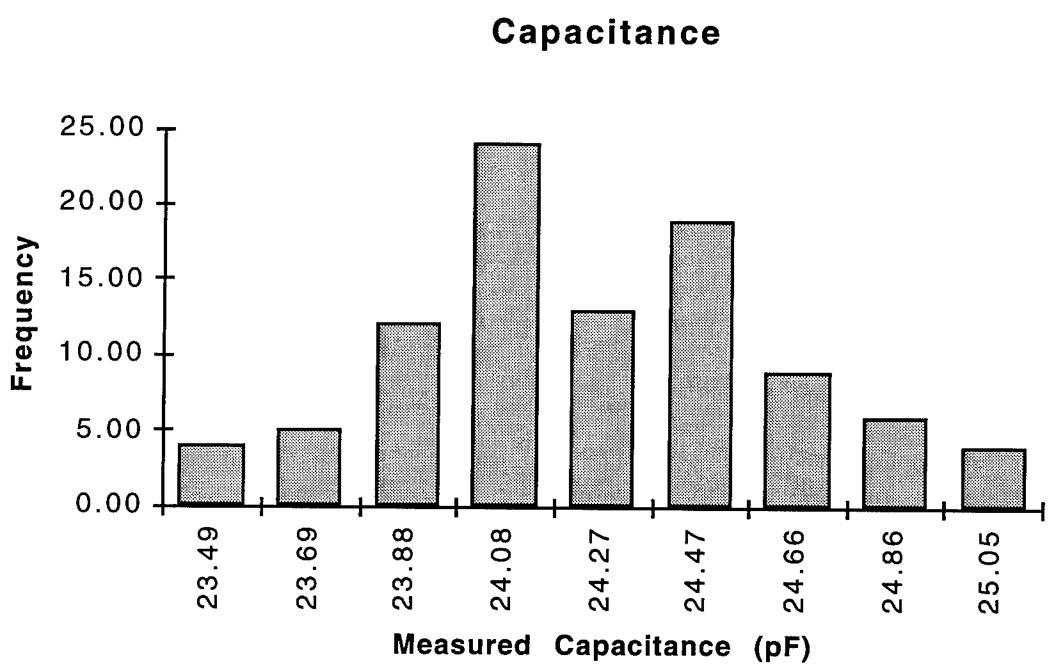

Figure 68. Censored Vendor B Wafer 1 measured capacitance.

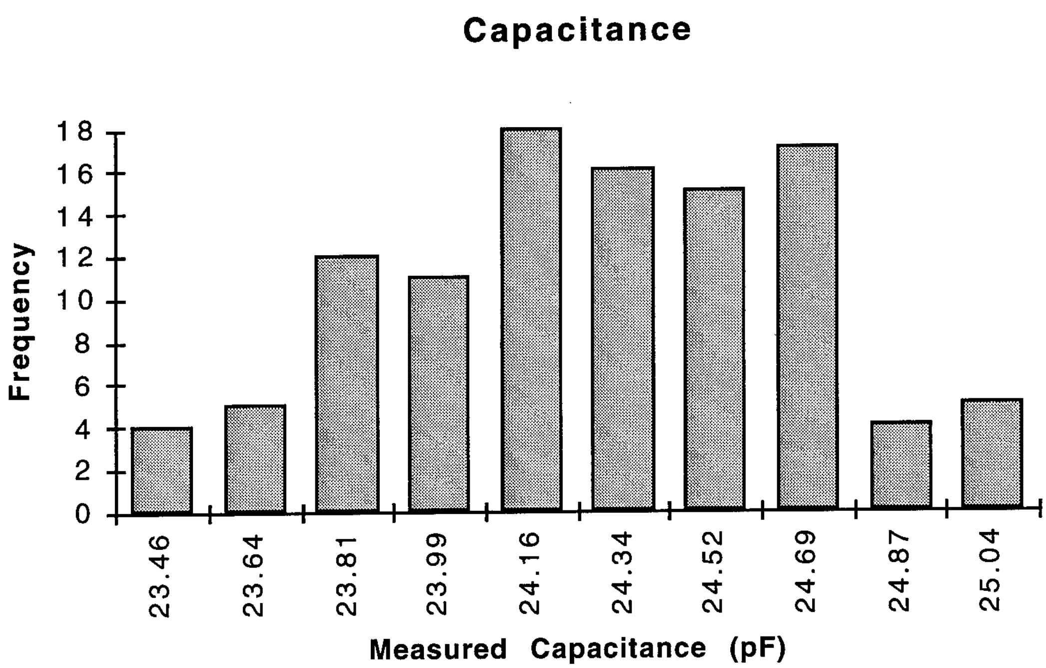

Figure 69. Uncensored Vendor B Wafer 2 measured capacitance.

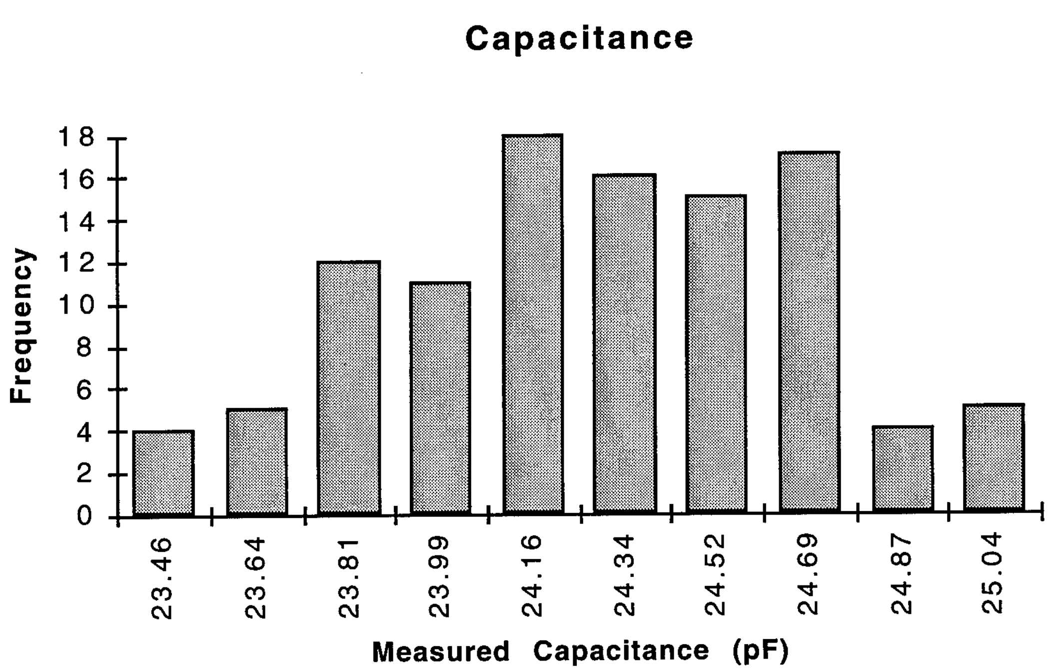

Figure 70. Censored Vendor B Wafer 2 measured capacitance.

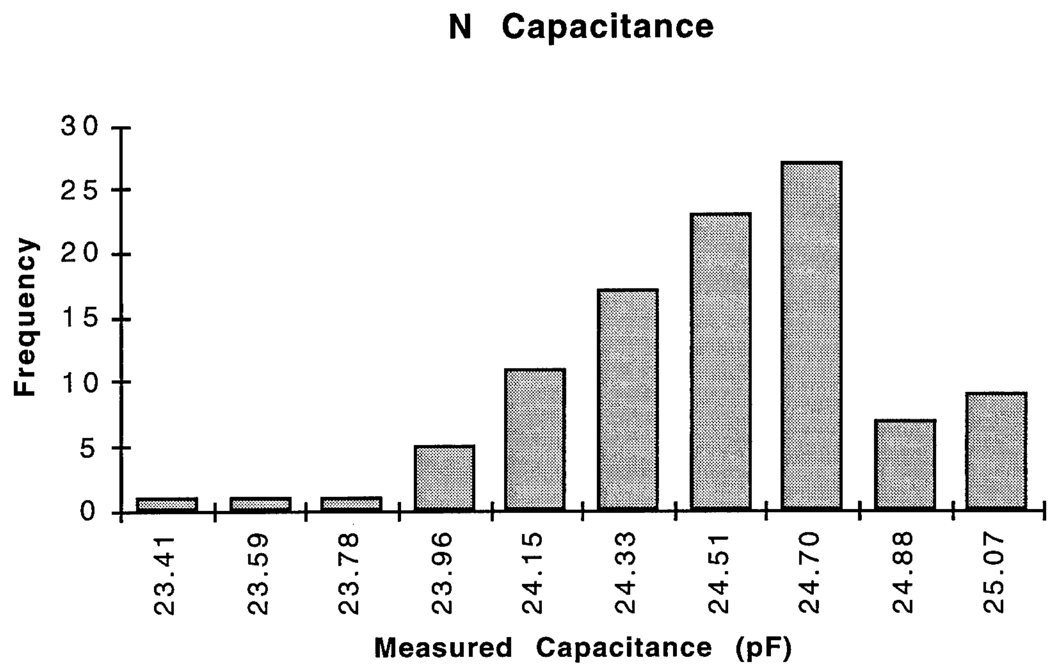

Figure 71. Uncensored Vendor B N structure measured capacitance.

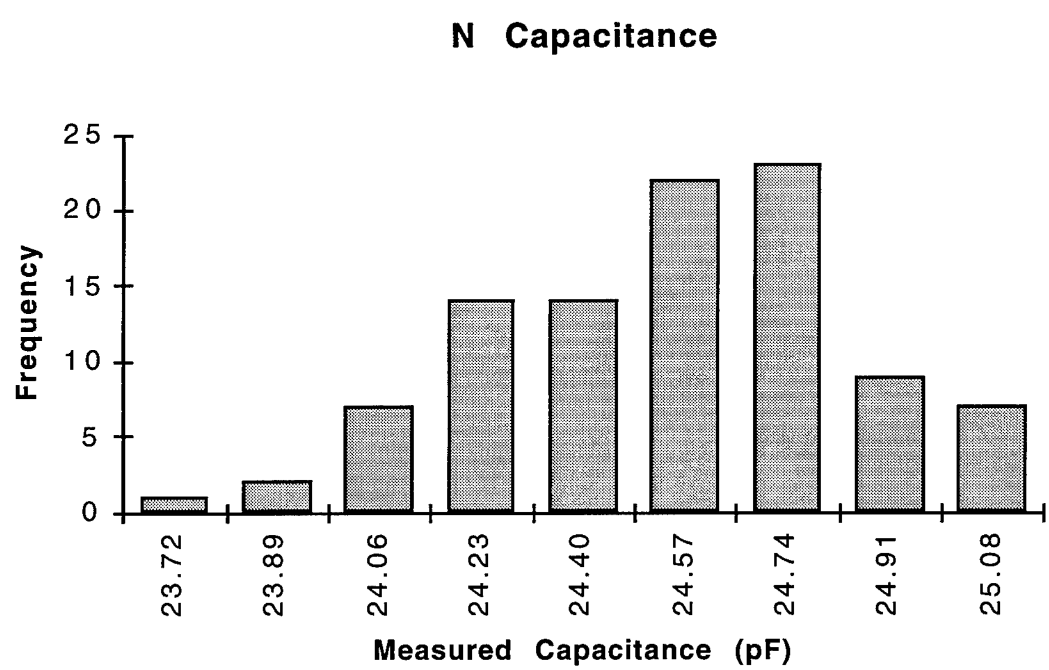

Figure 72. Censored Vendor B N structure measured capacitance.

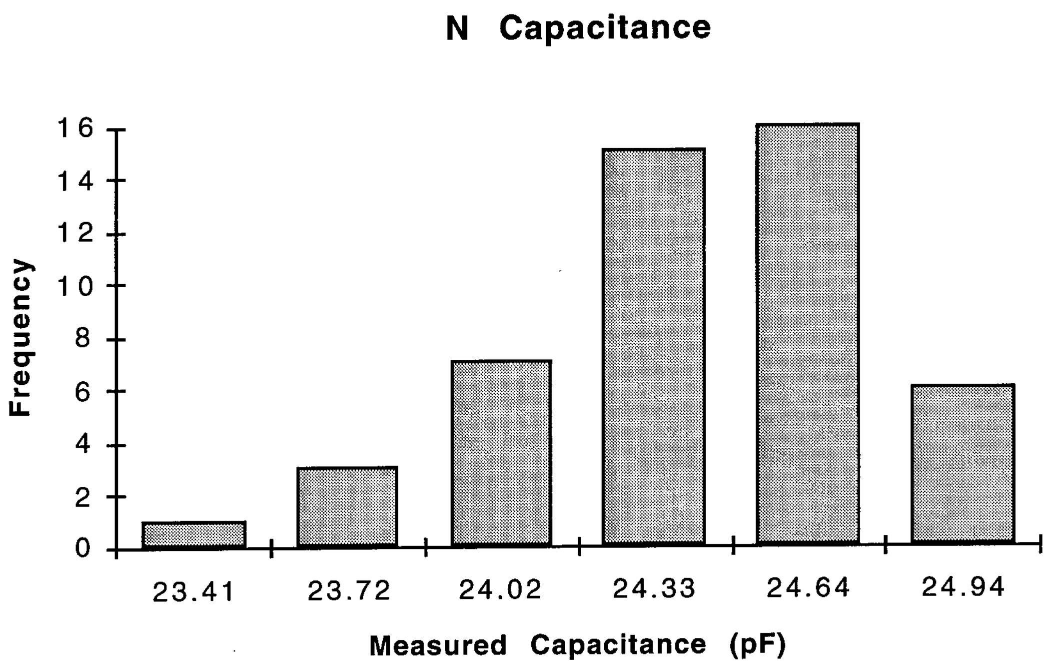

Figure 73. Uncensored Vendor B Wafer 1 N structure measured capacitance.

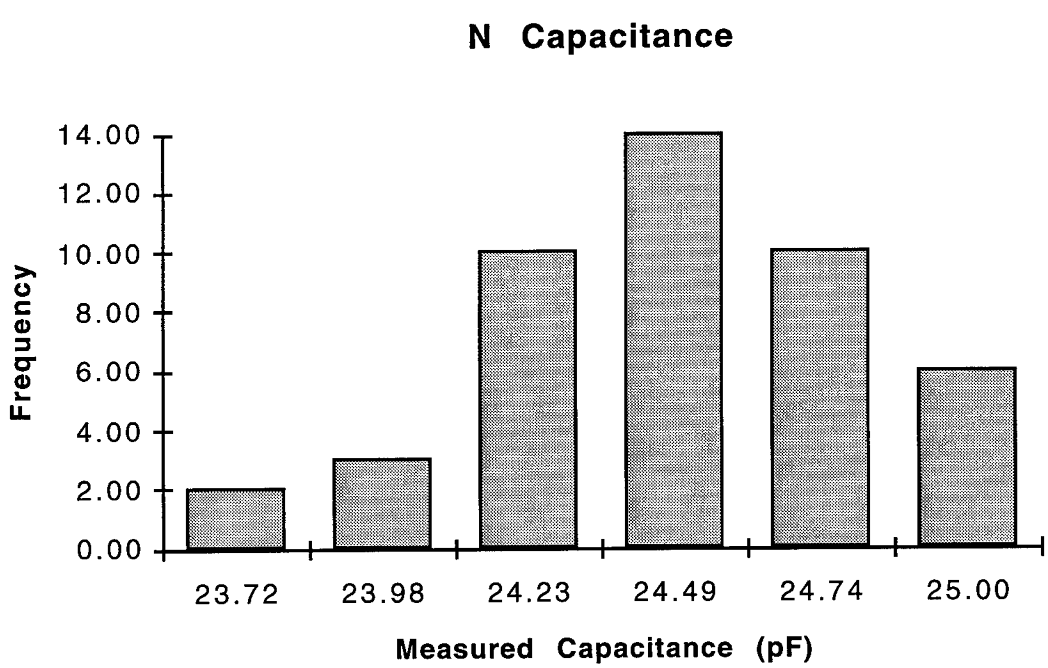

Figure 74. Censored Vendor B Wafer 1 N structure measured capacitance.

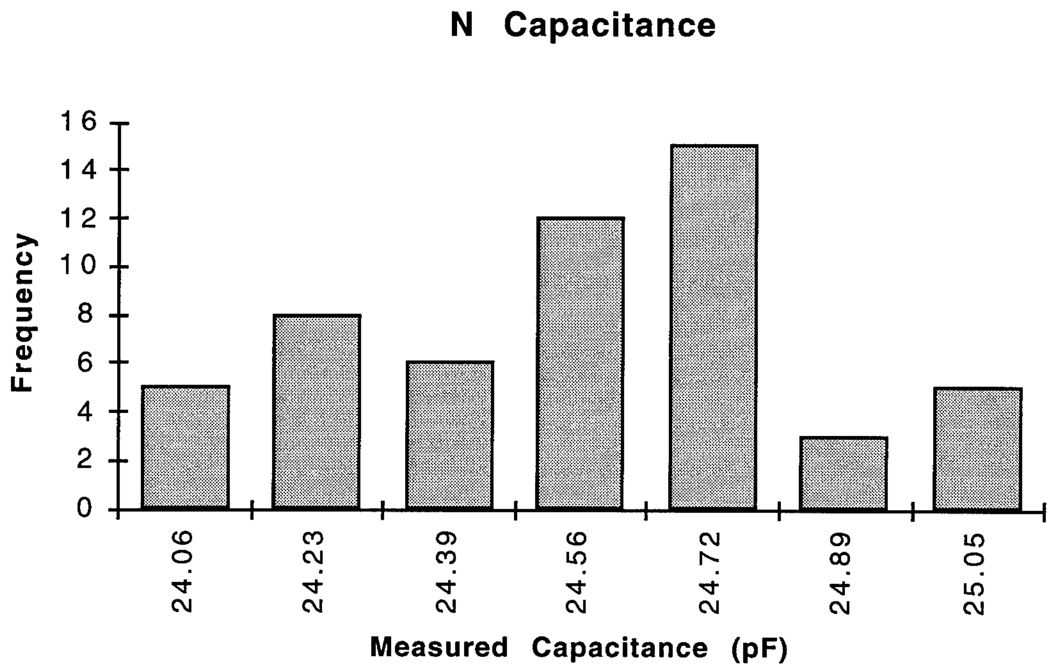

Figure 75. Uncensored Vendor B Wafer 2 N structure measured capacitance.

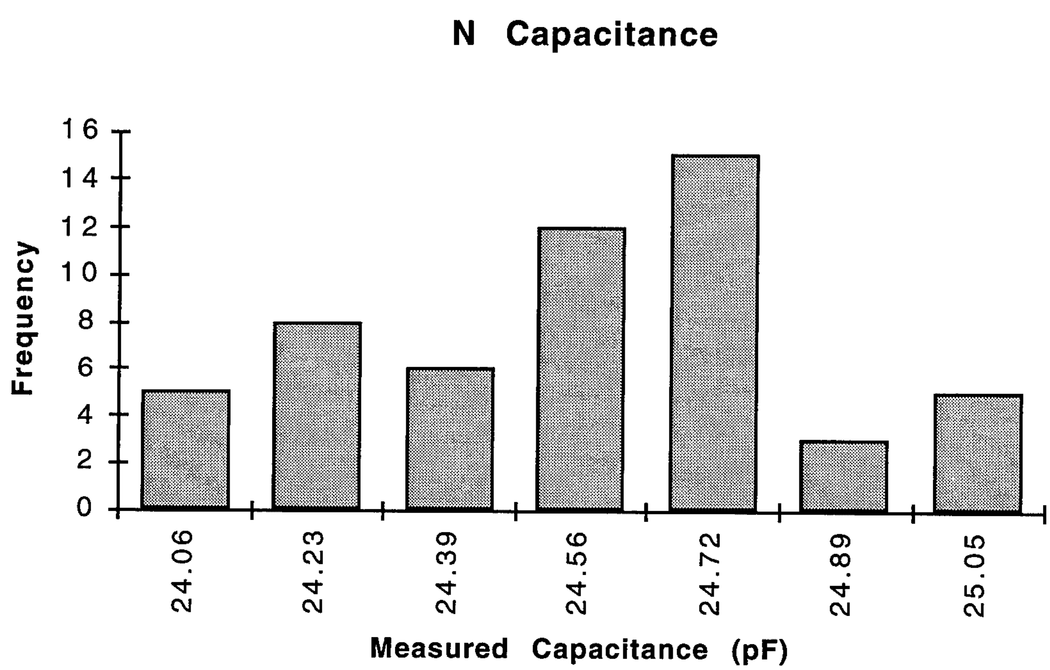

Figure 76. Censored Vendor B Wafer 2 N structure measured capacitance.

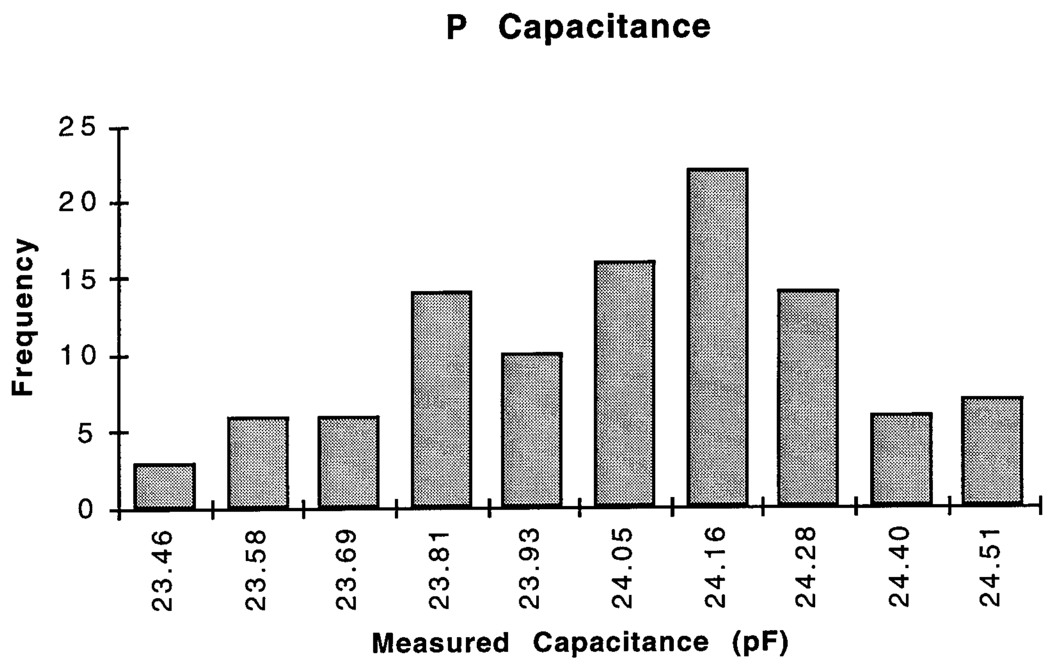

Figure 77. Uncensored Vendor B P structure measured capacitance.

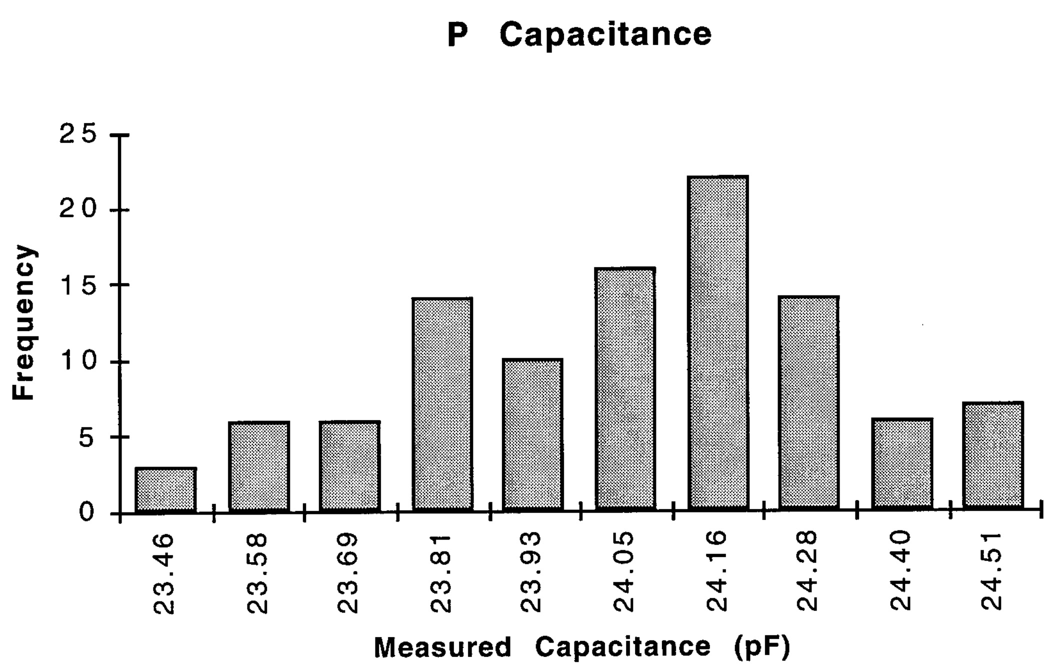

Figure 78. Censored Vendor B P structure measured capacitance.

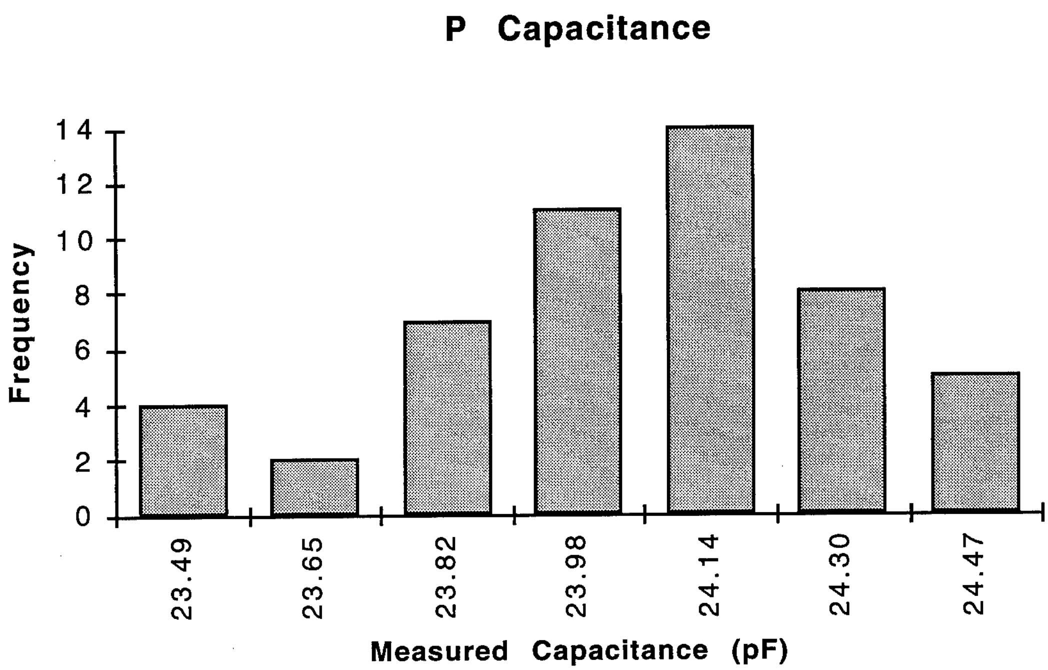

Figure 79. Uncensored Vendor B Wafer 1 P structure measured capacitance.

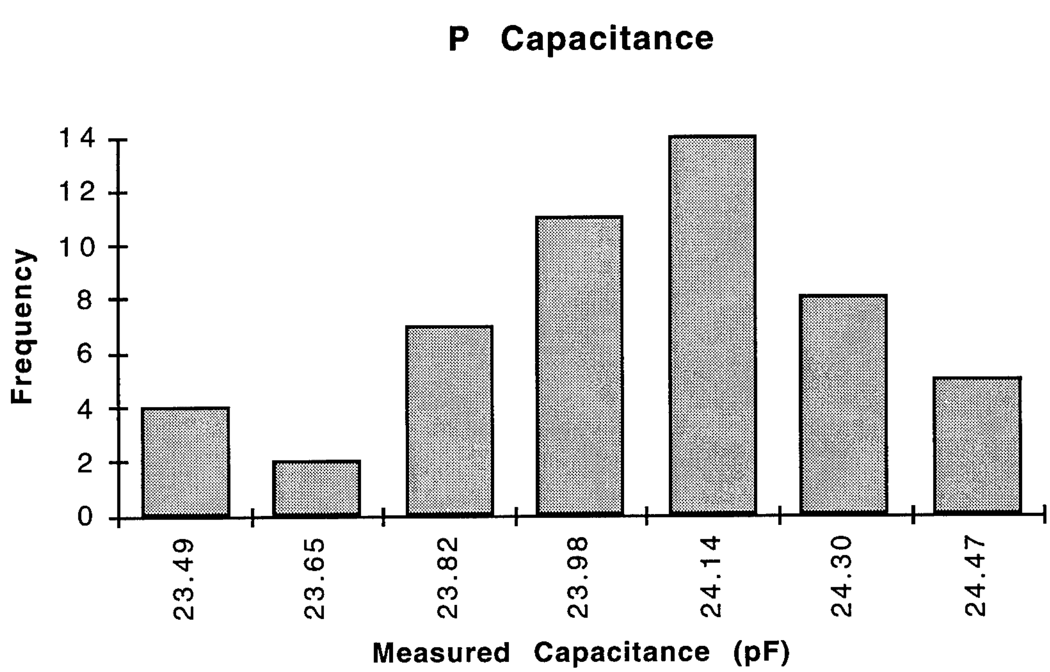

Figure 80. Censored Vendor B Wafer 1 P structure measured capacitance.

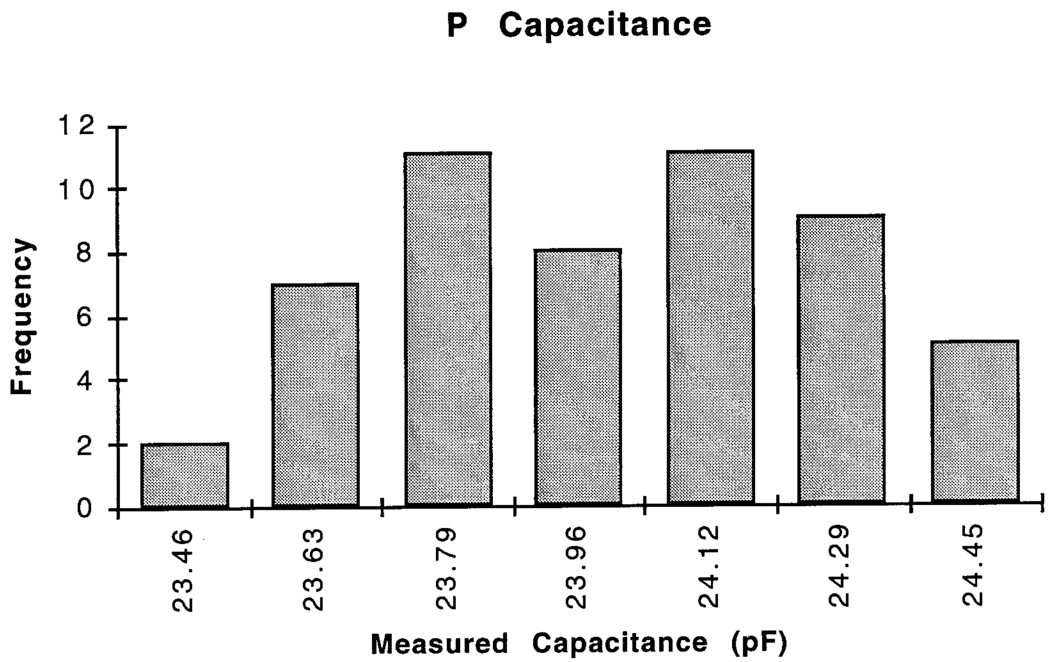

Figure 81. Uncensored Vendor B Wafer 2 P structure measured capacitance.

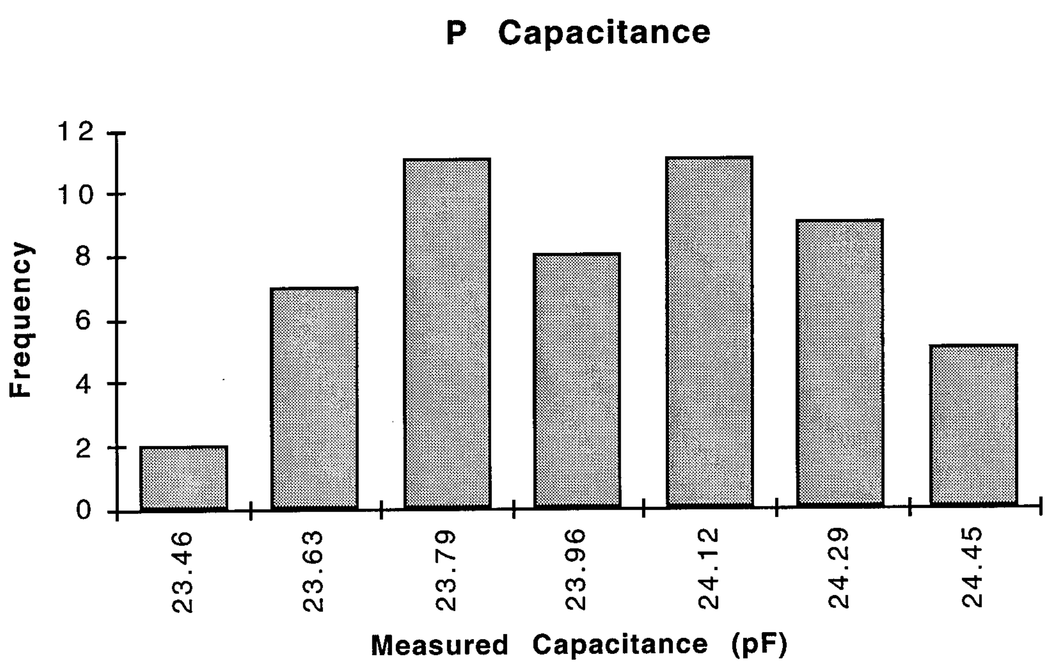

Figure 82. Censored Vendor B Wafer 2 P structure measured capacitance.

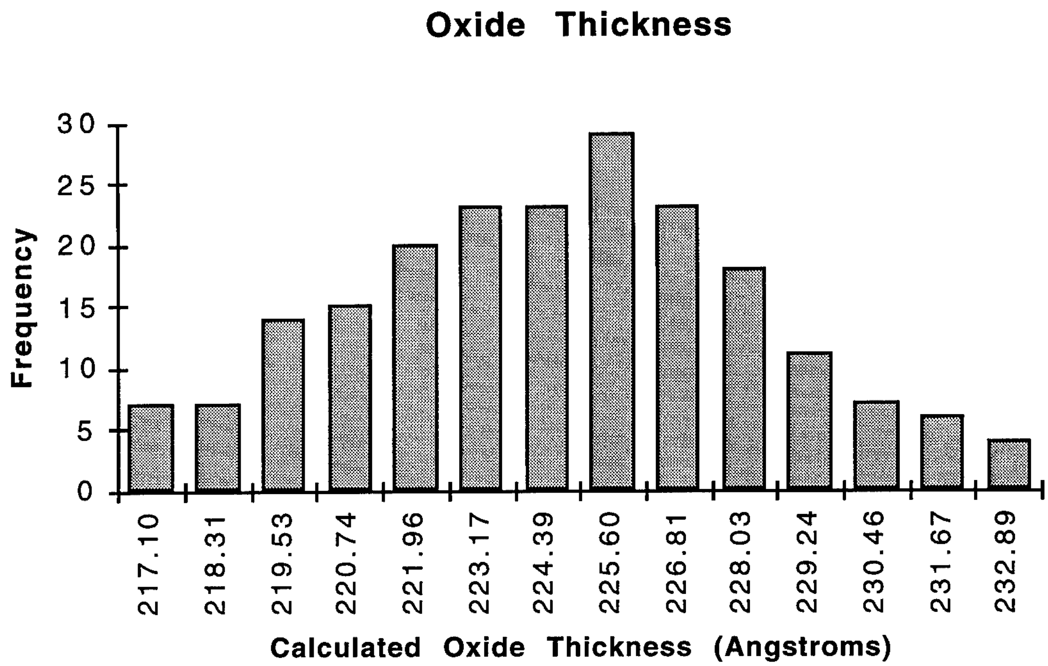

Figure 83. Uncensored Vendor B calculated oxide thickness.

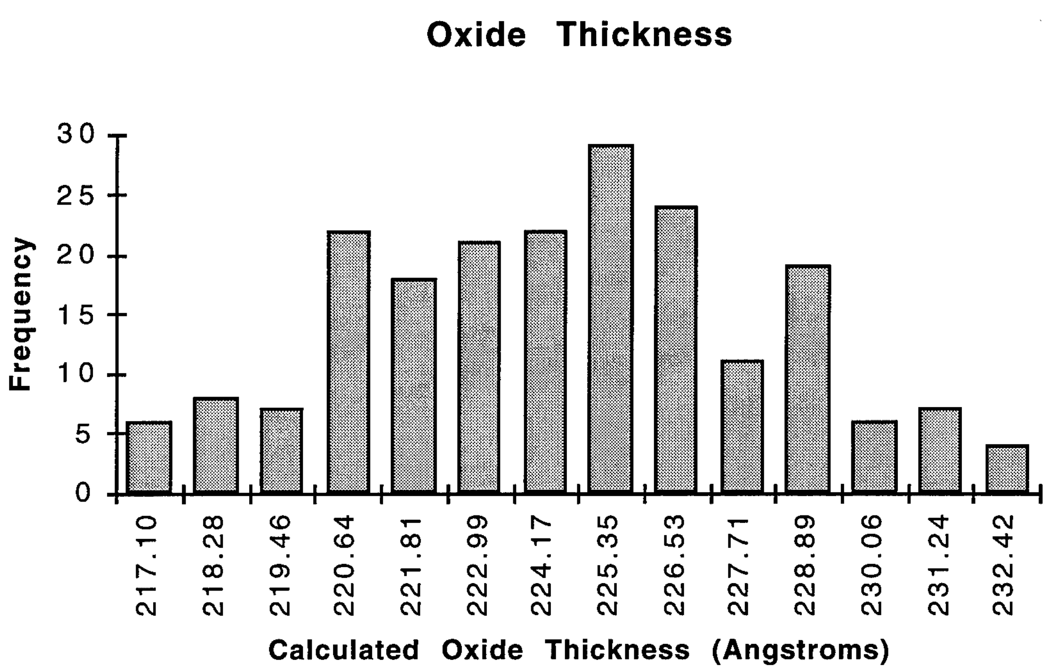

Figure 84. Censored Vendor B calculated oxide thickness.

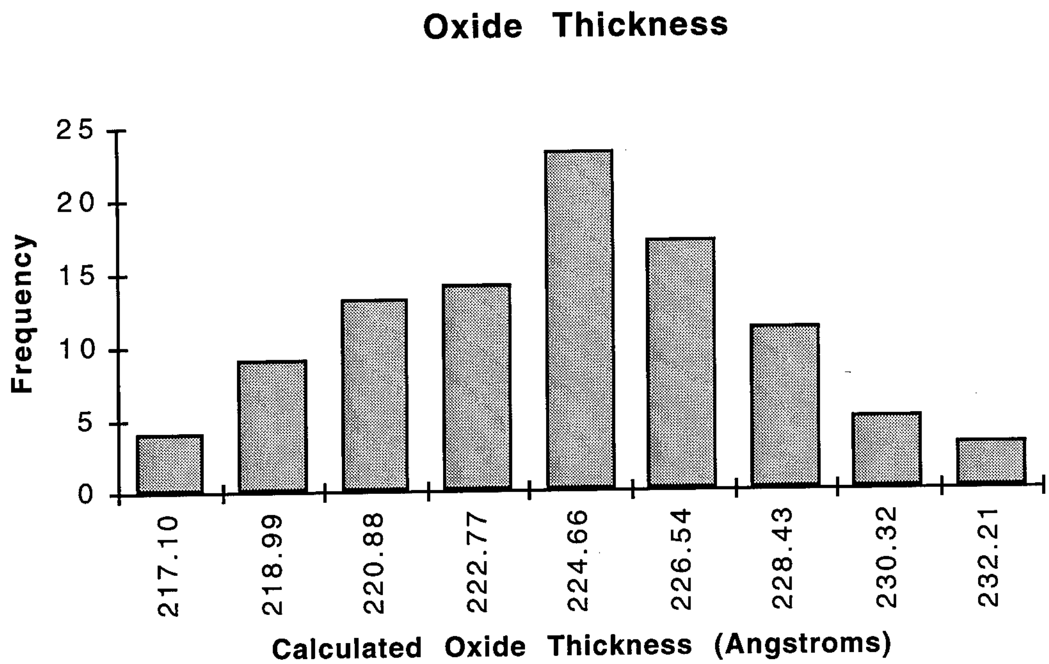

Figure 85. Uncensored Vendor B Wafer 1 calculated oxide thickness.

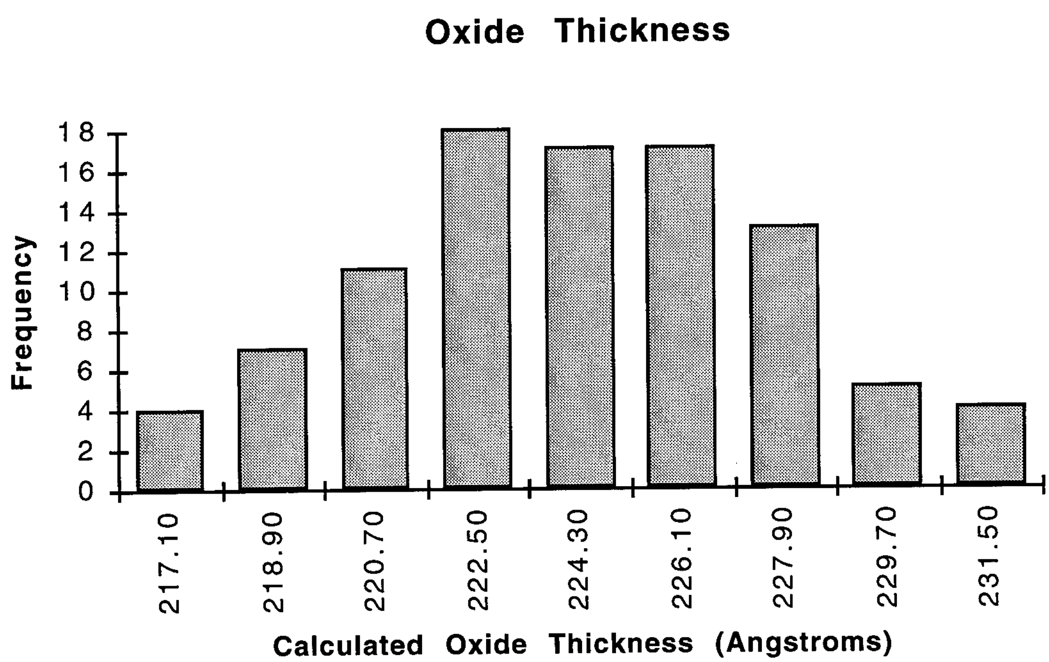

Figure 86. Censored Vendor B Wafer 1 calculated oxide thickness.

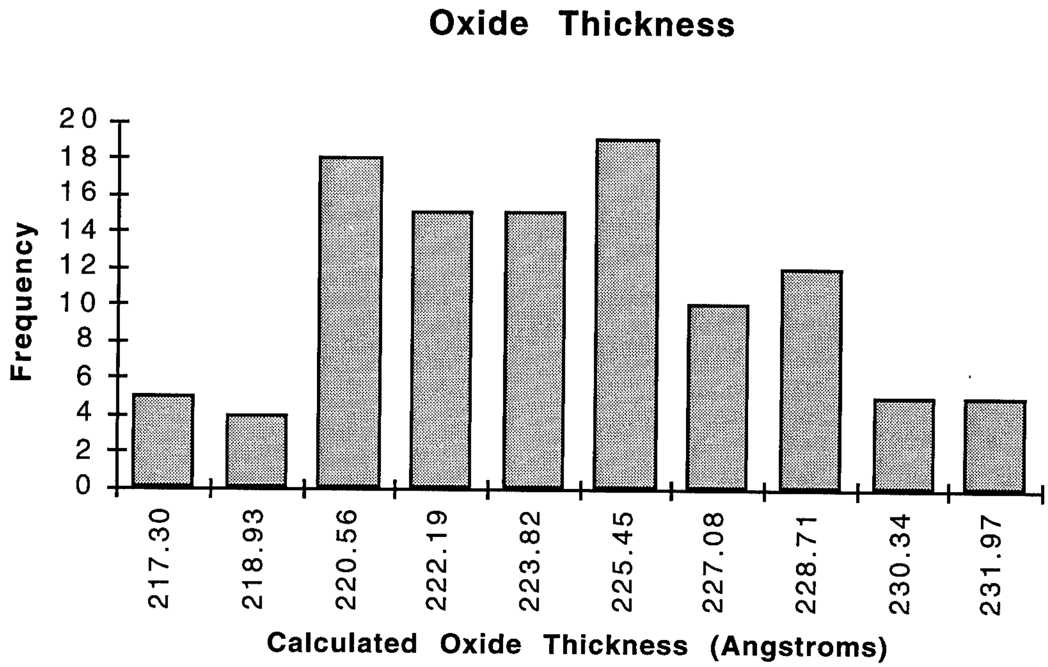

Figure 87. Censored Vendor B Wafer 2 calculated oxide thickness.

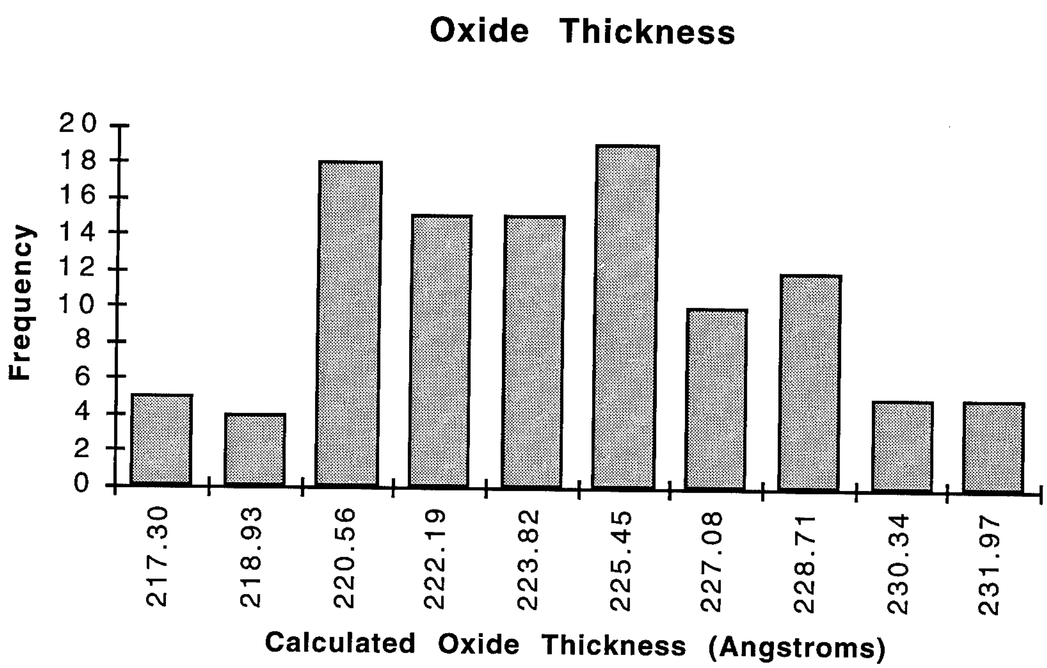

Figure 88. Uncensored Vendor B Wafer 2 calculated oxide thickness.

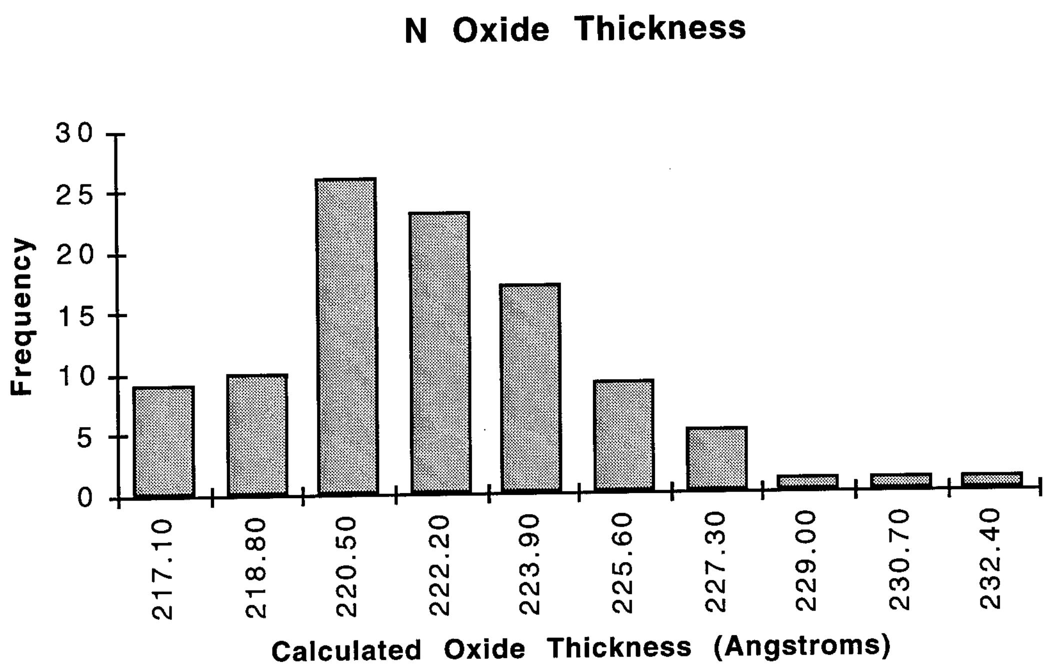

Figure 89. Uncensored Vendor B N structure calculated oxide thickness.

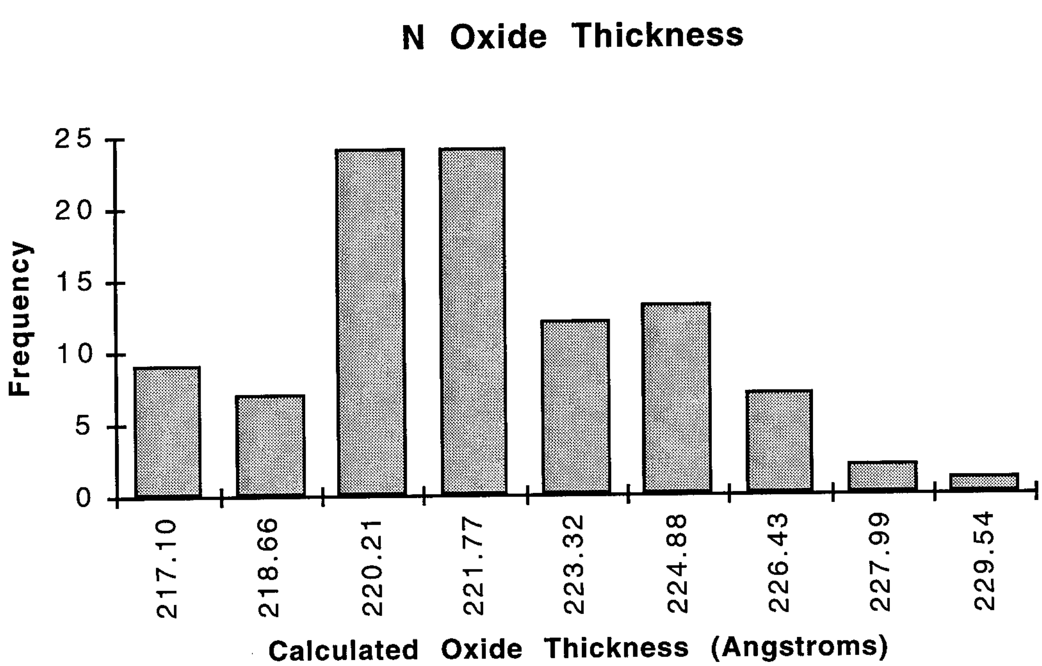

Figure 90. Censored Vendor B N structure calculated oxide thickness.

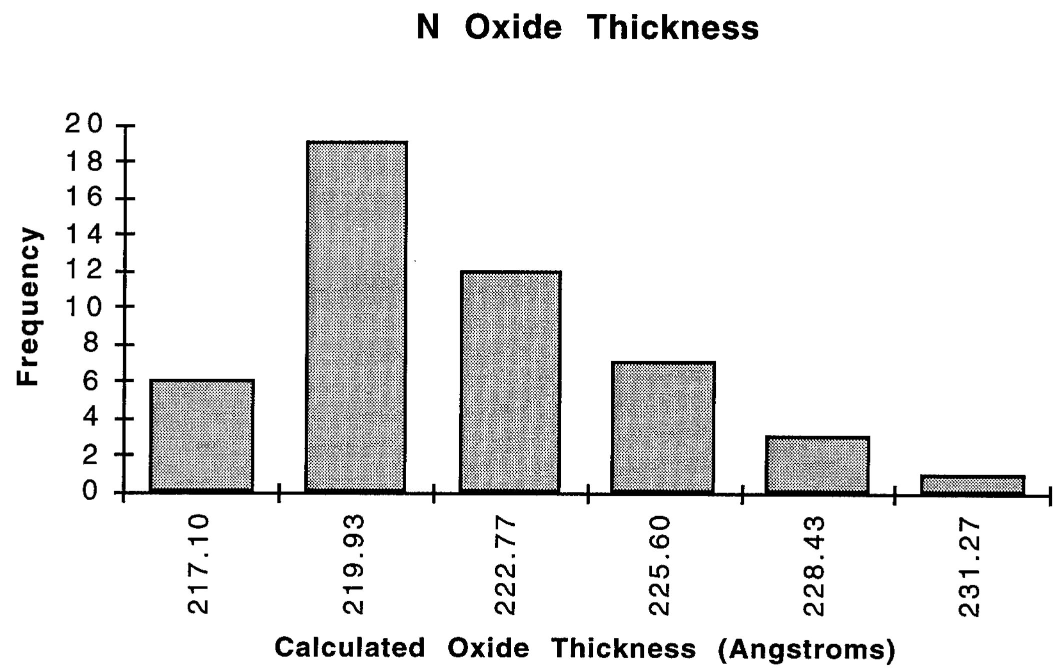

Figure 91. Uncensored Vendor B Wafer 1 N structure calculated oxide thickness.

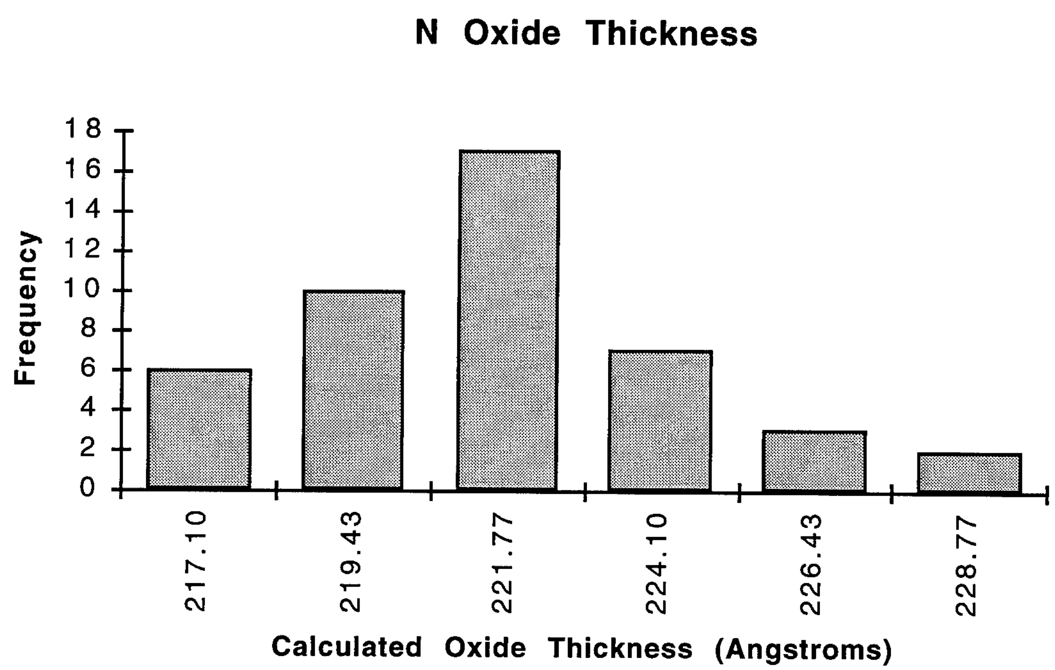

Figure 92. Censored Vendor B Wafer 1 N structure calculated oxide thickness.

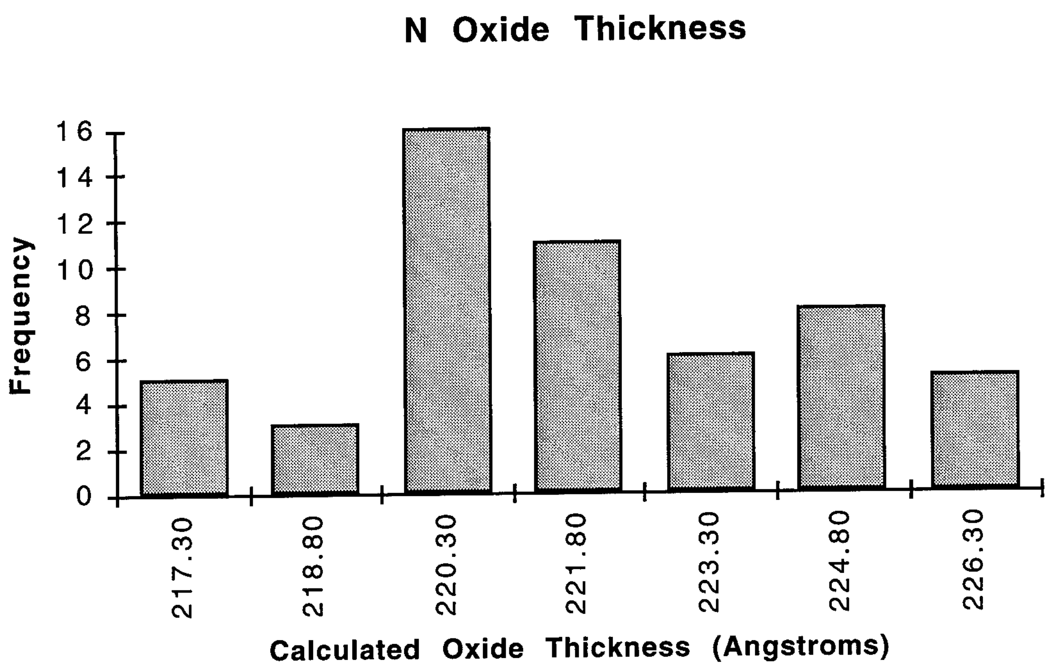

Figure 93. Uncensored Vendor B Wafer 2 N structure calculated oxide thickness.

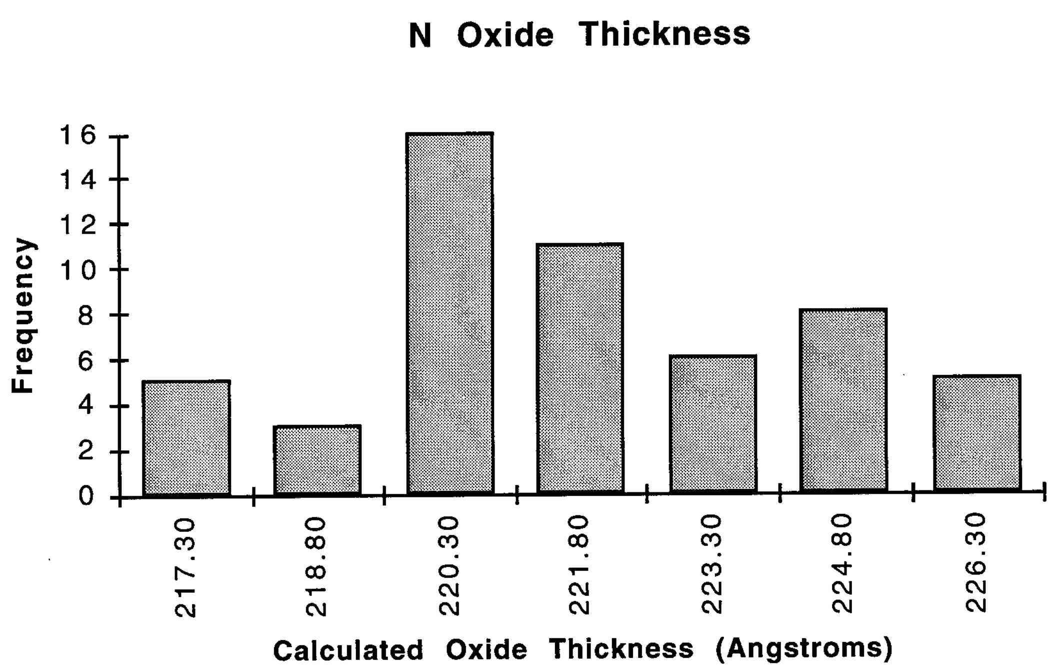

Figure 94. Censored Vendor B Wafer 2 N structure calculated oxide thickness.

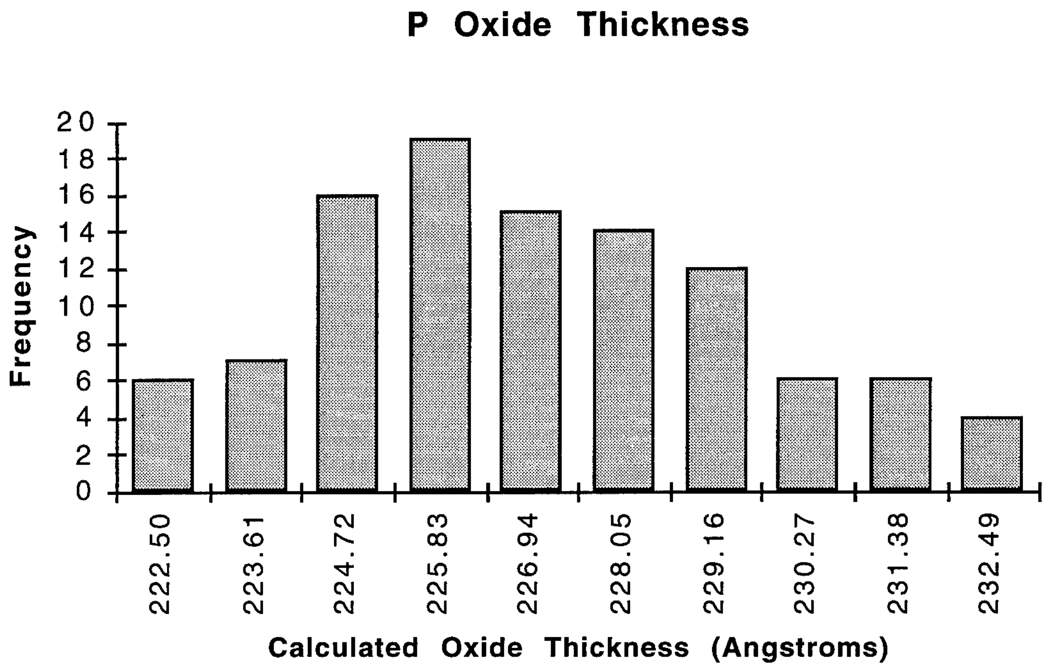

Figure 95. Uncensored Vendor B P structure calculated oxide thickness.

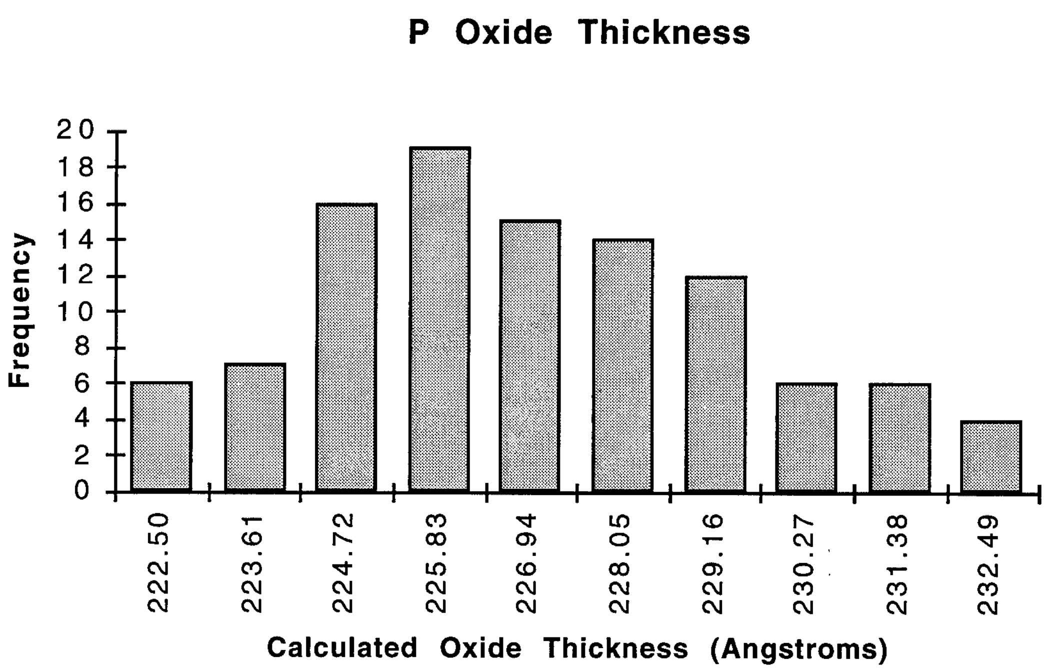

Figure 96. Censored Vendor B P structure calculated oxide thickness.

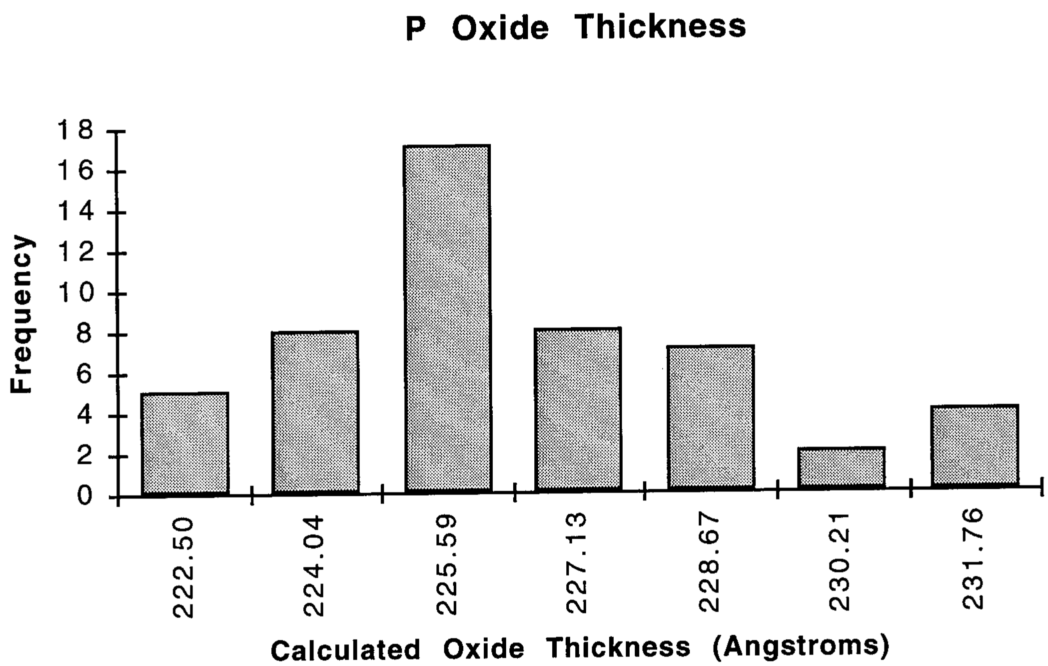

Figure 97. Uncensored Vendor B Wafer 1 P structure calculated oxide thickness.

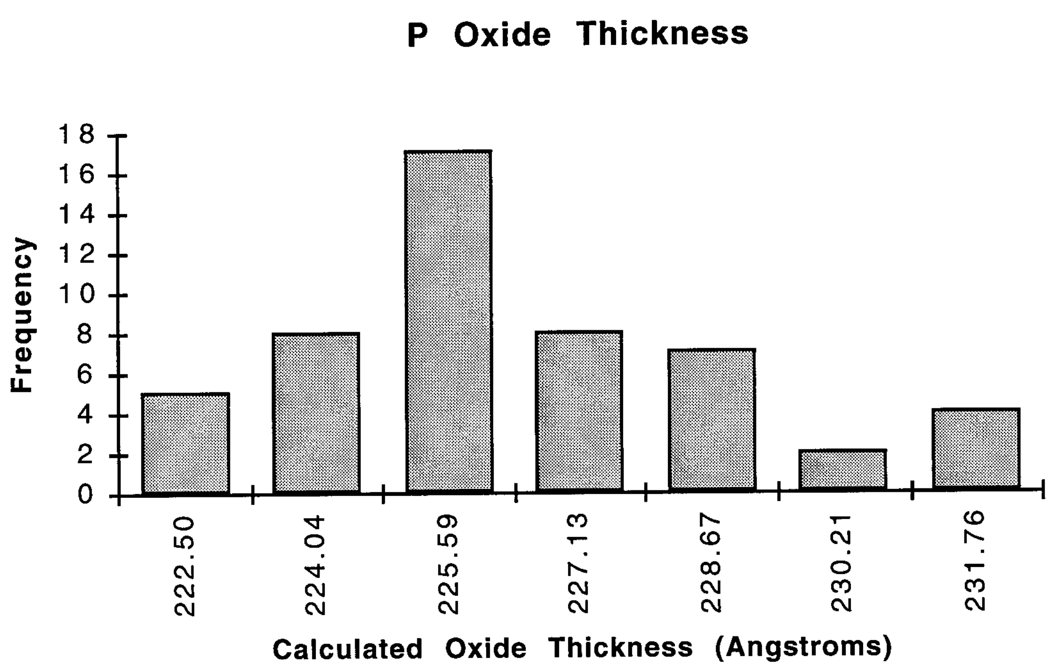

Figure 98. Censored Vendor B Wafer 1 P structure calculated oxide thickness.

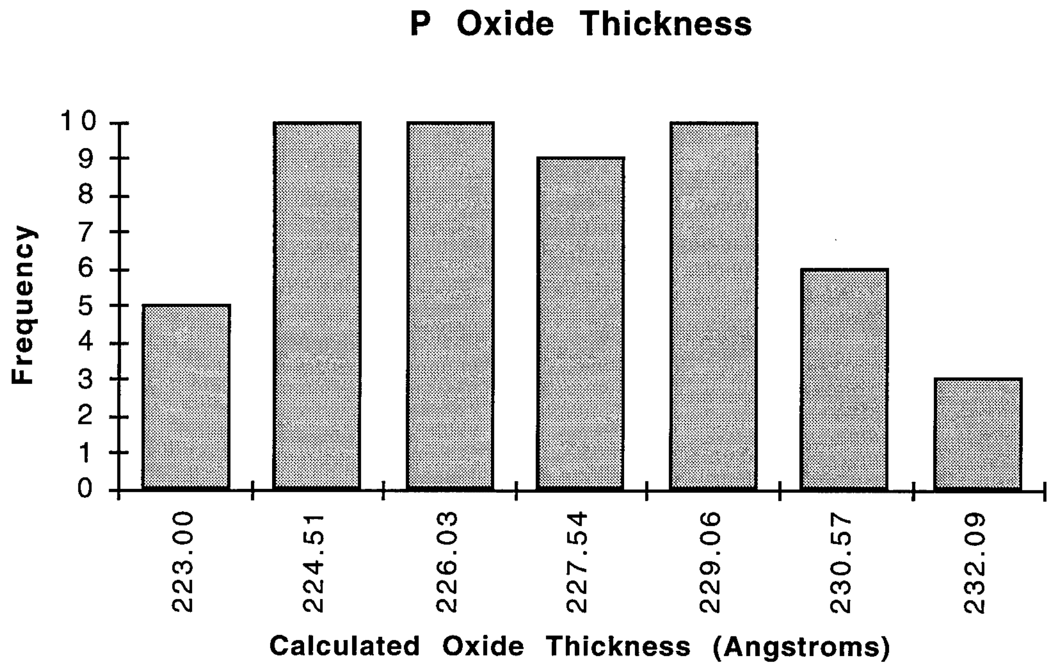

Figure 99. Uncensored Vendor B Wafer 2 P structure calculated oxide thickness.

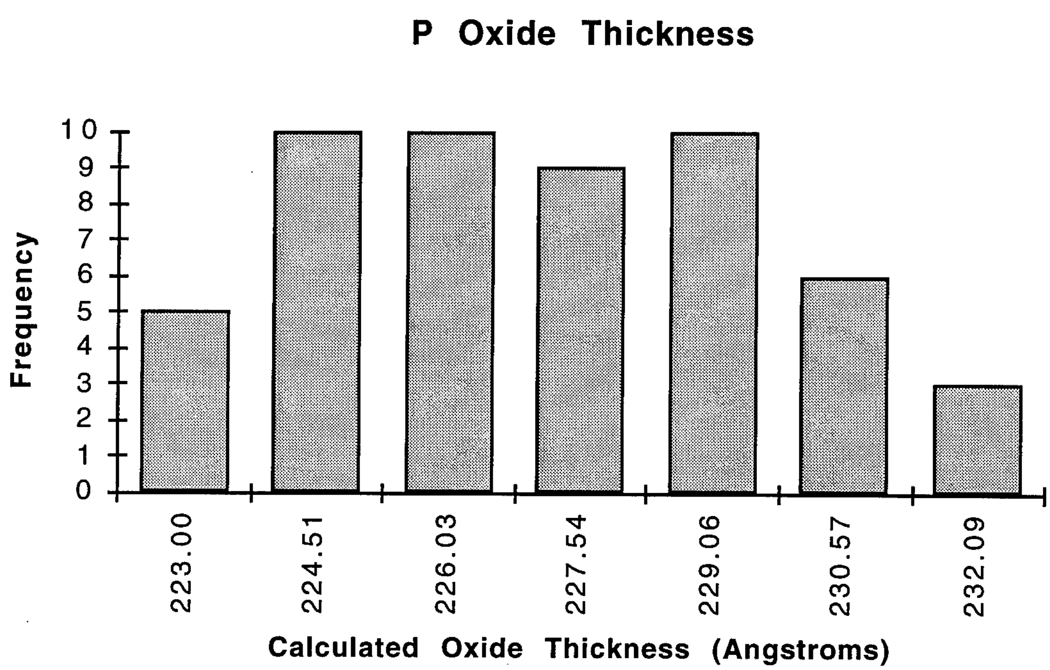

Figure 100. Censored Vendor B Wafer 2 P structure calculated oxide thickness.

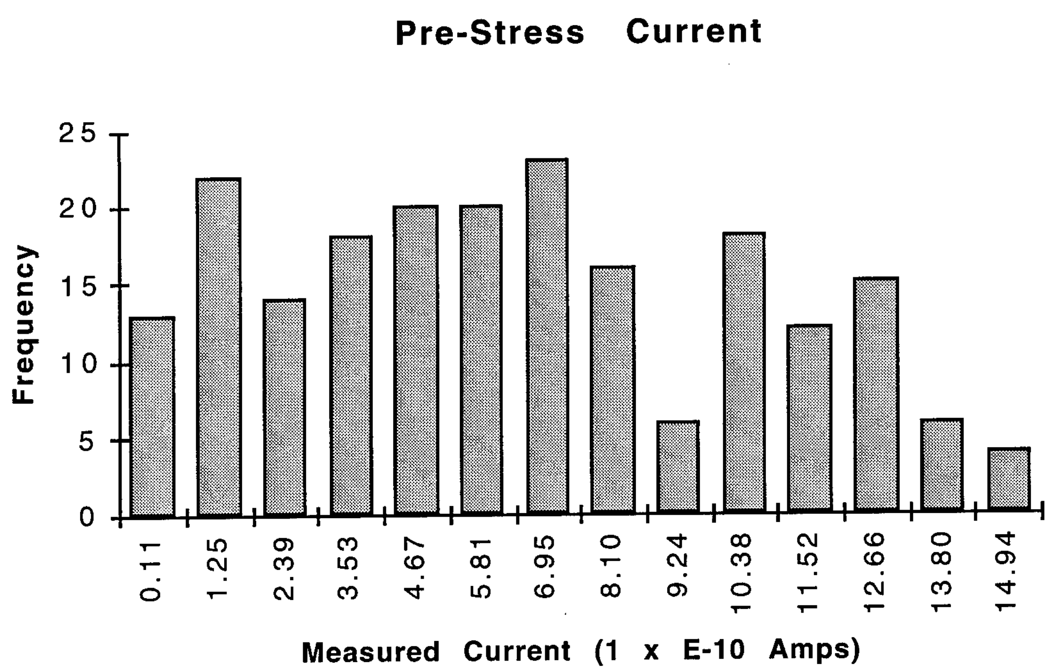

Figure 101. Uncensored Vendor B measured initial current.

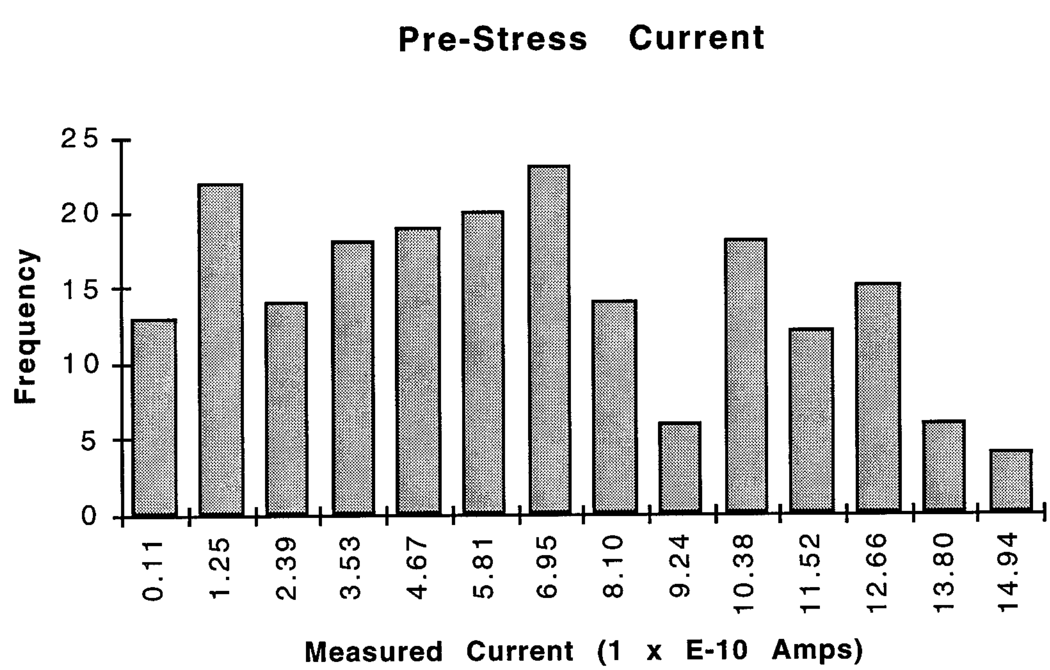

Figure 102. Censored Vendor B measured initial current.

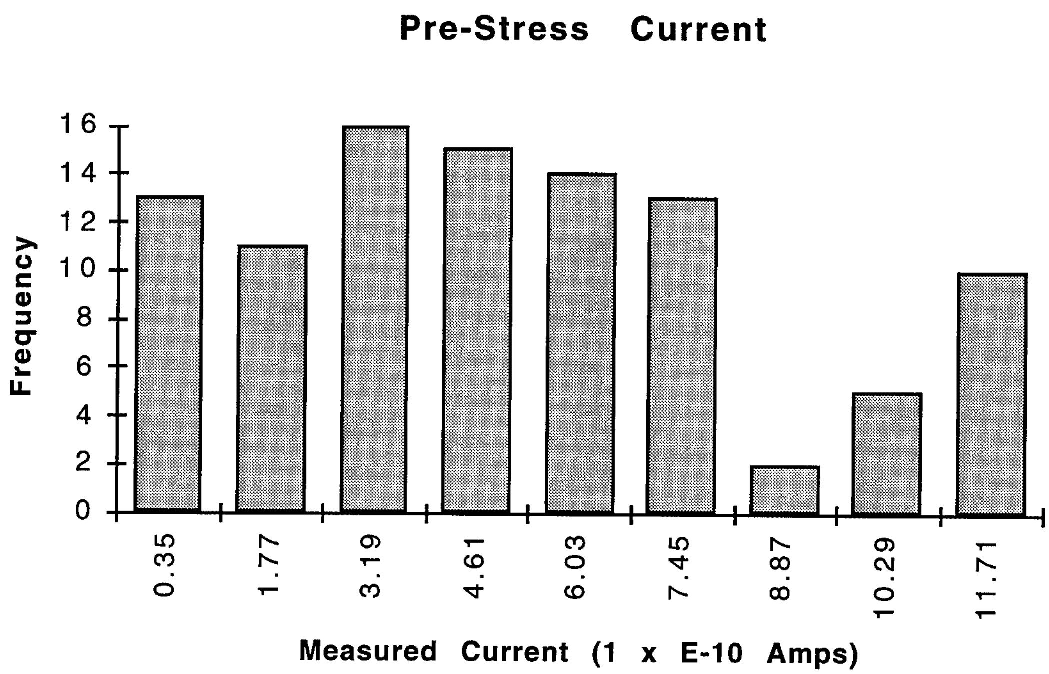

Figure 103. Uncensored Vendor B Wafer 1 measured initial current.

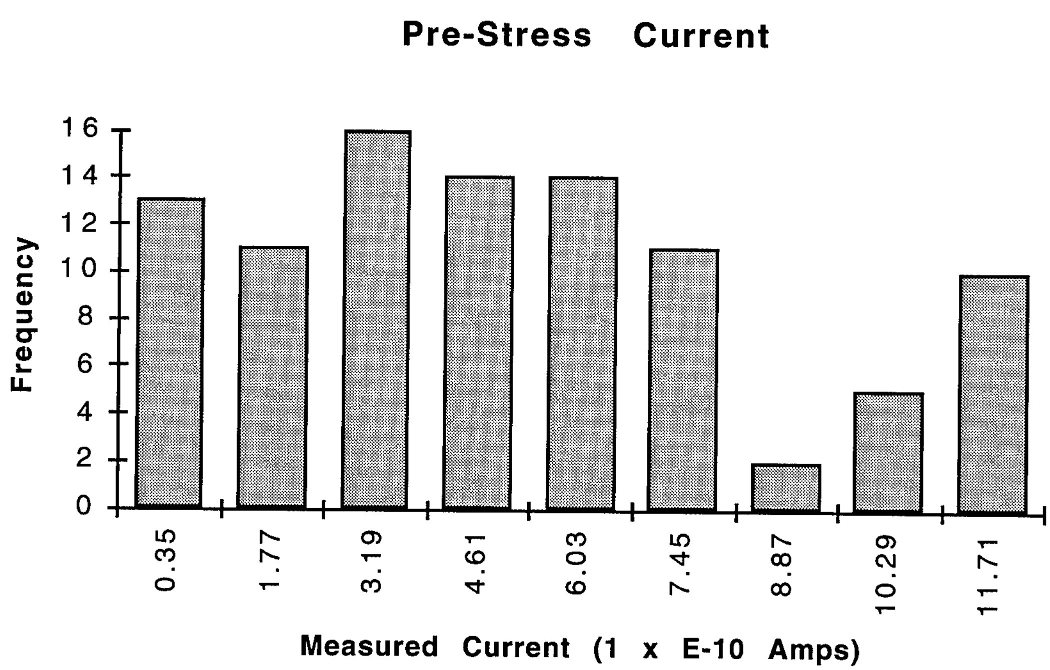

Figure 104. Censored Vendor B Wafer 1 measured initial current.

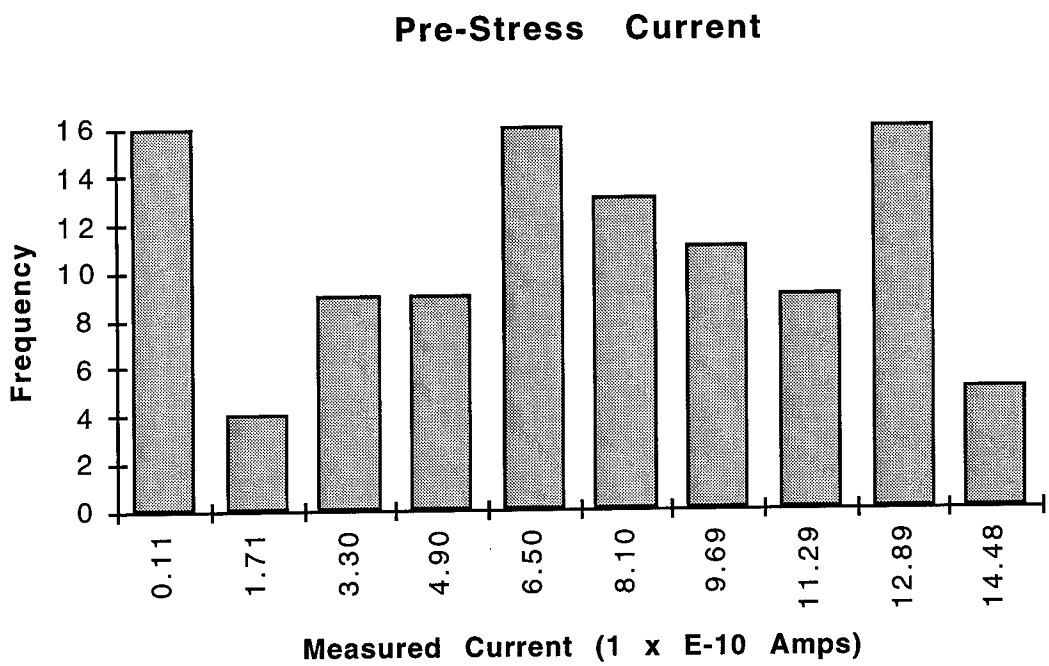

Figure 105. Uncensored Vendor B Wafer 2 measured initial current.

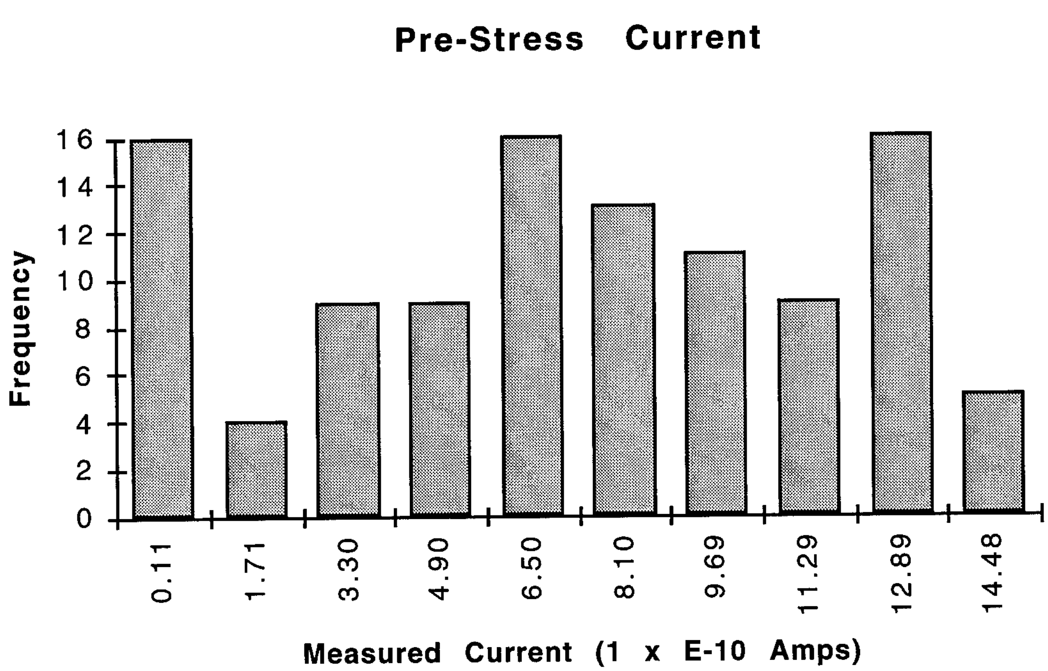

Figure 106. Censored Vendor B Wafer 2 measured initial current.

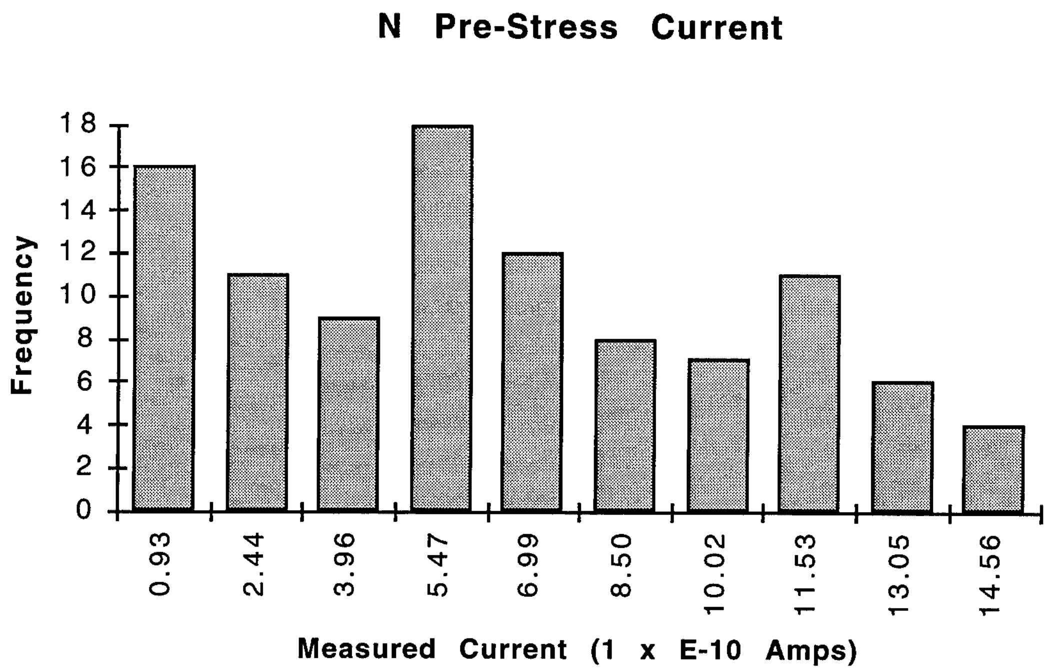

Figure 107. Uncensored Vendor B N structure measured initial current.

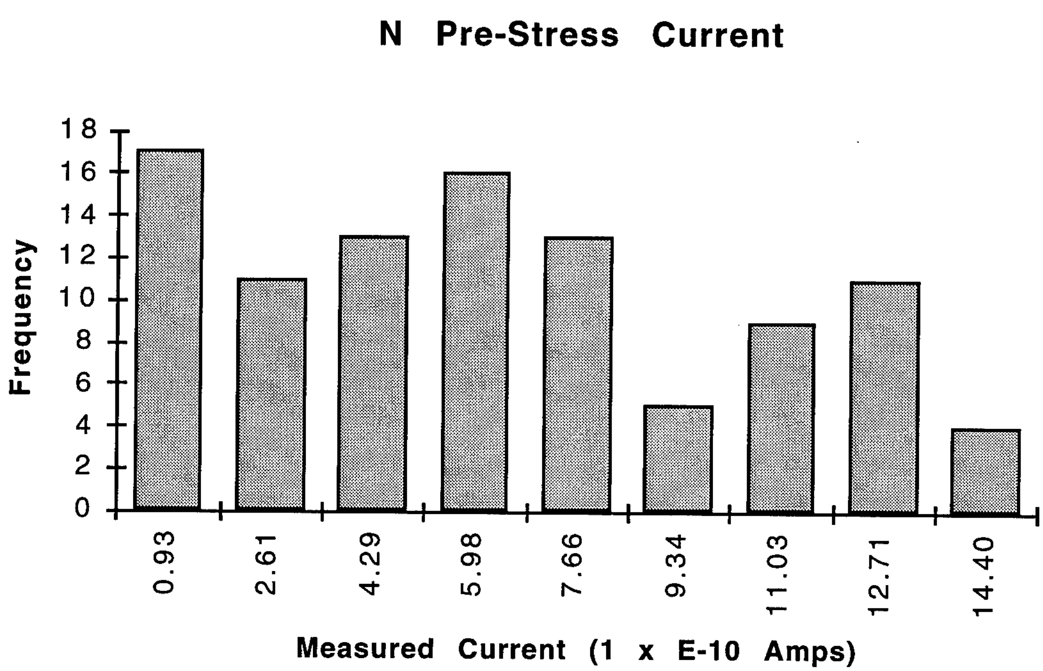

Figure 108. Censored Vendor B N structure measured initial current.

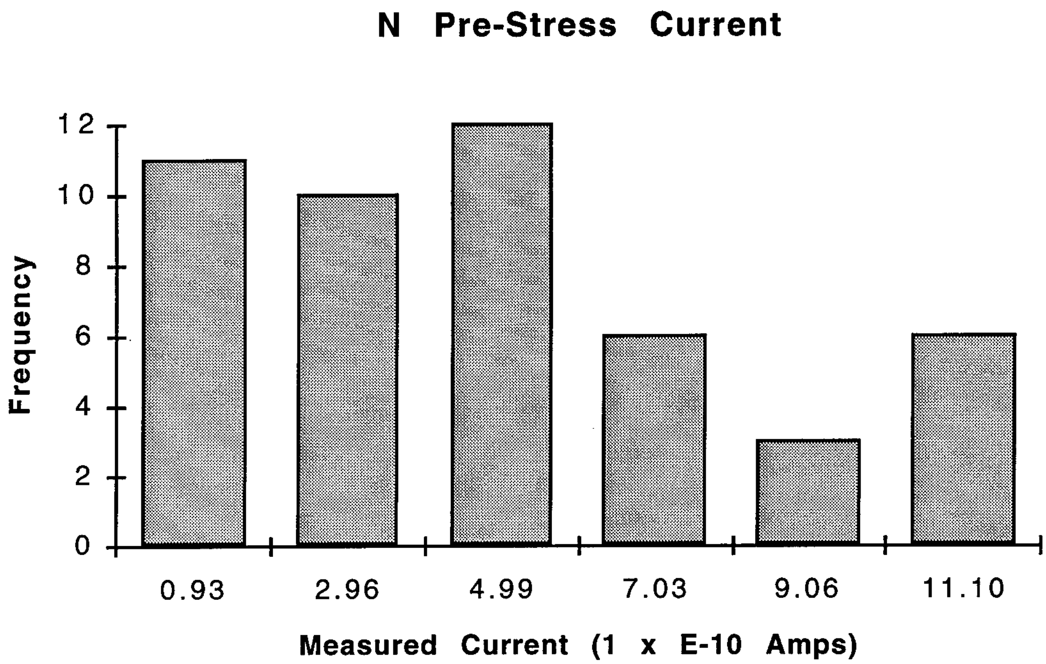

Figure 109. Uncensored Vendor B Wafer 1 N structure measured initial current.

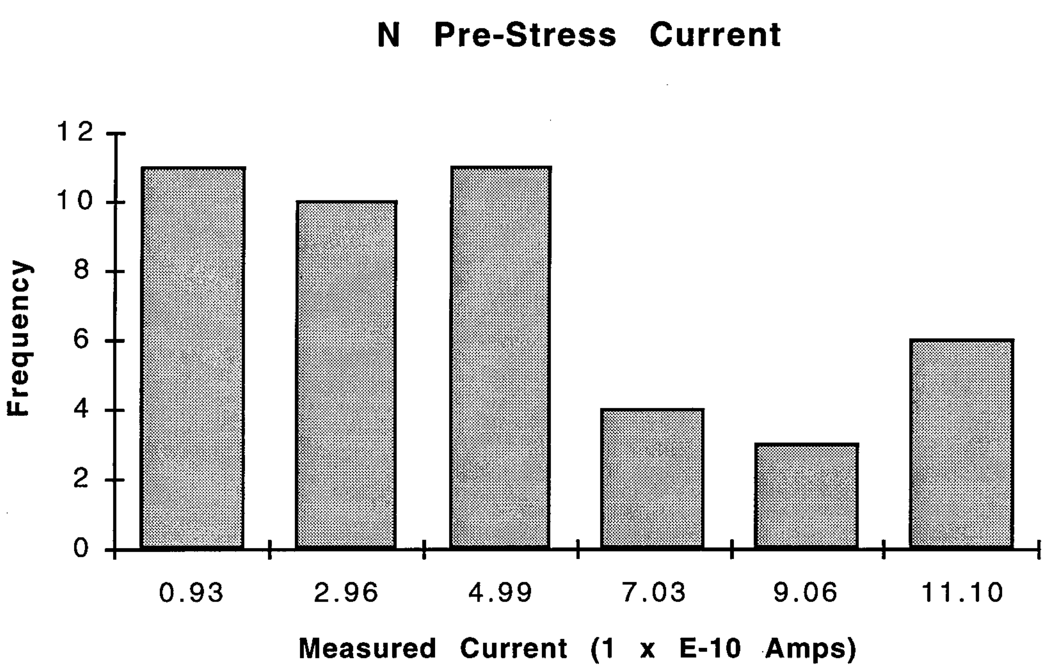

Figure 110. Censored Vendor B Wafer 1 N structure measured initial current.

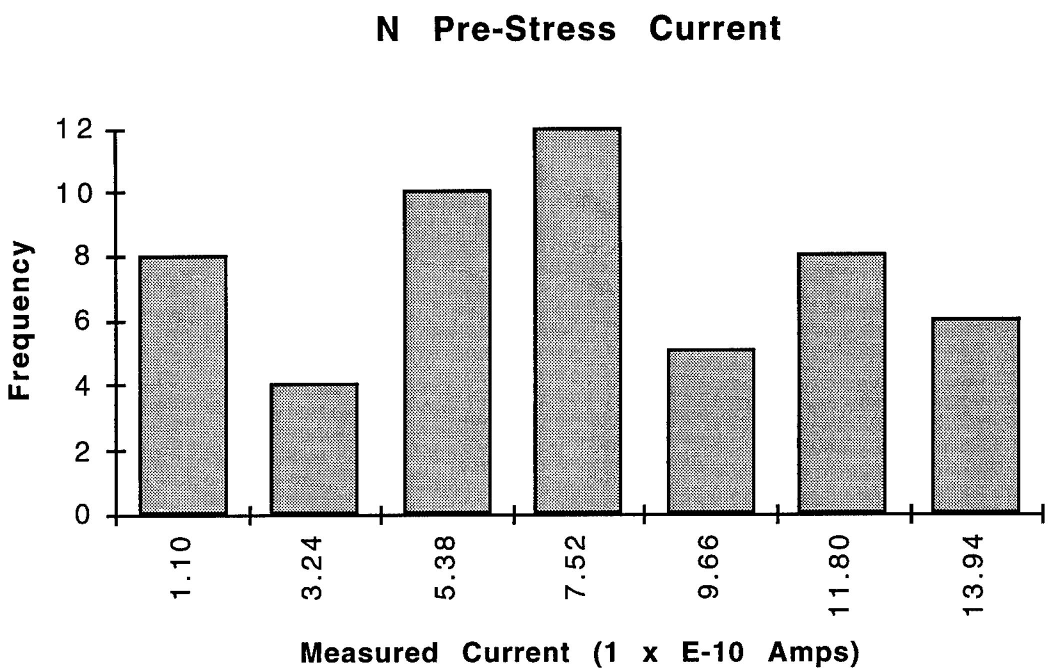

Figure 111. Uncensored Vendor B Wafer 2 N structure measured initial current.

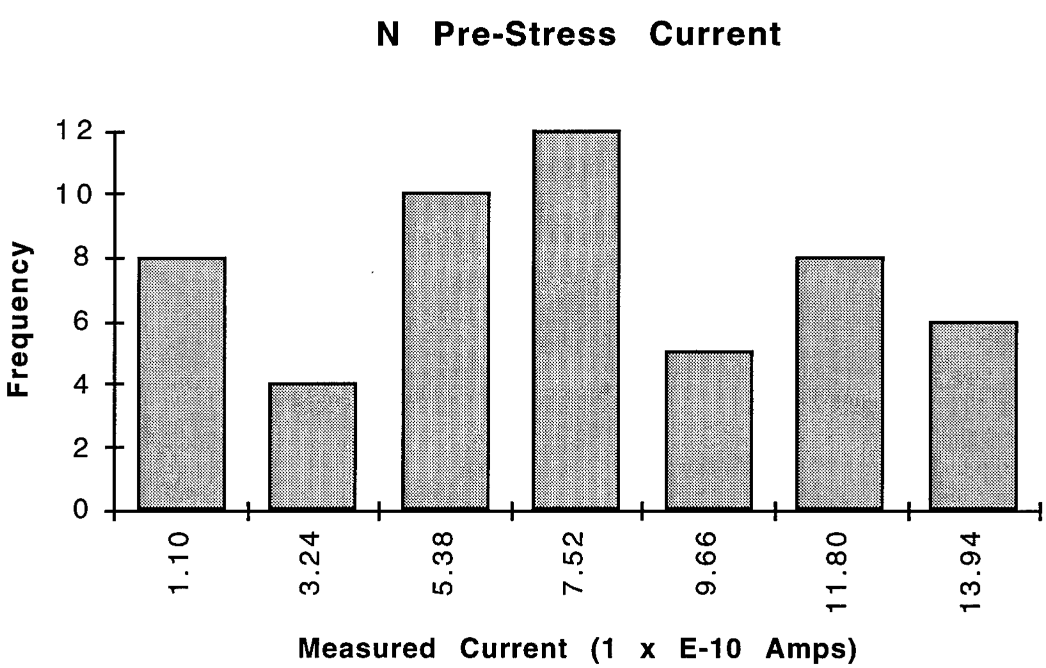

Figure 112. Censored Vendor B Wafer 2 N structure measured initial current.

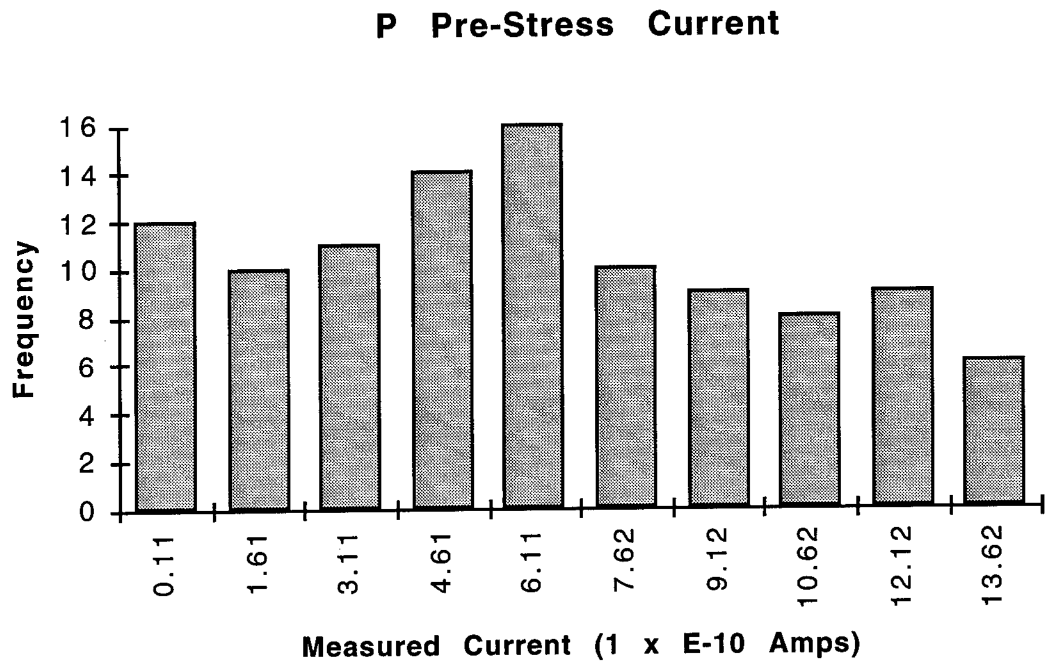

Figure 113. Uncensored Vendor B P structure measured initial current.

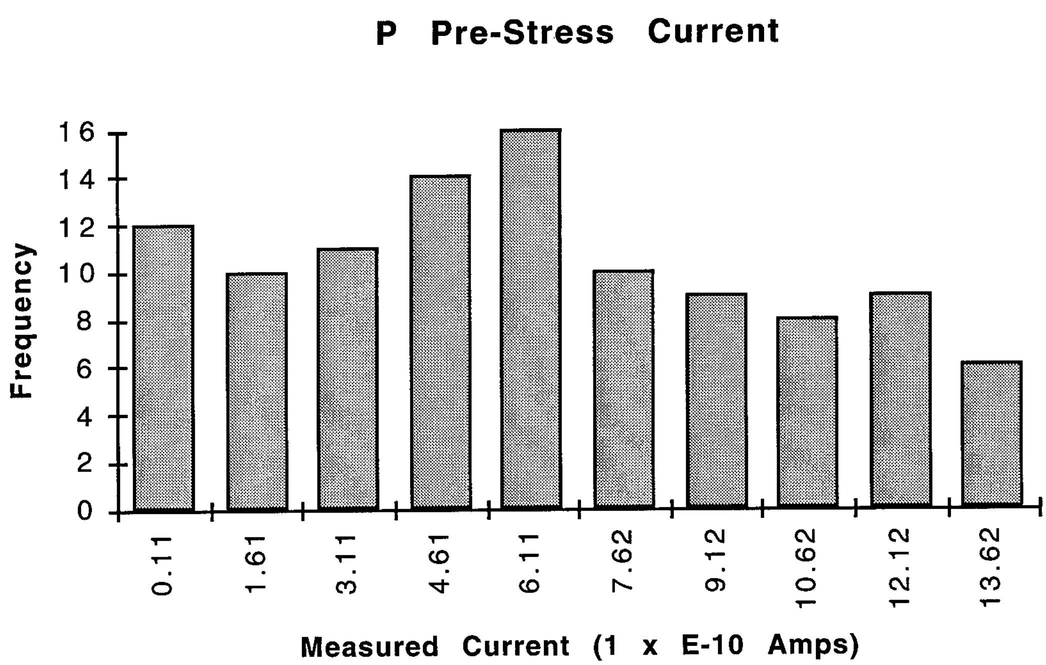

Figure 114. Censored Vendor B P structure measured initial current.

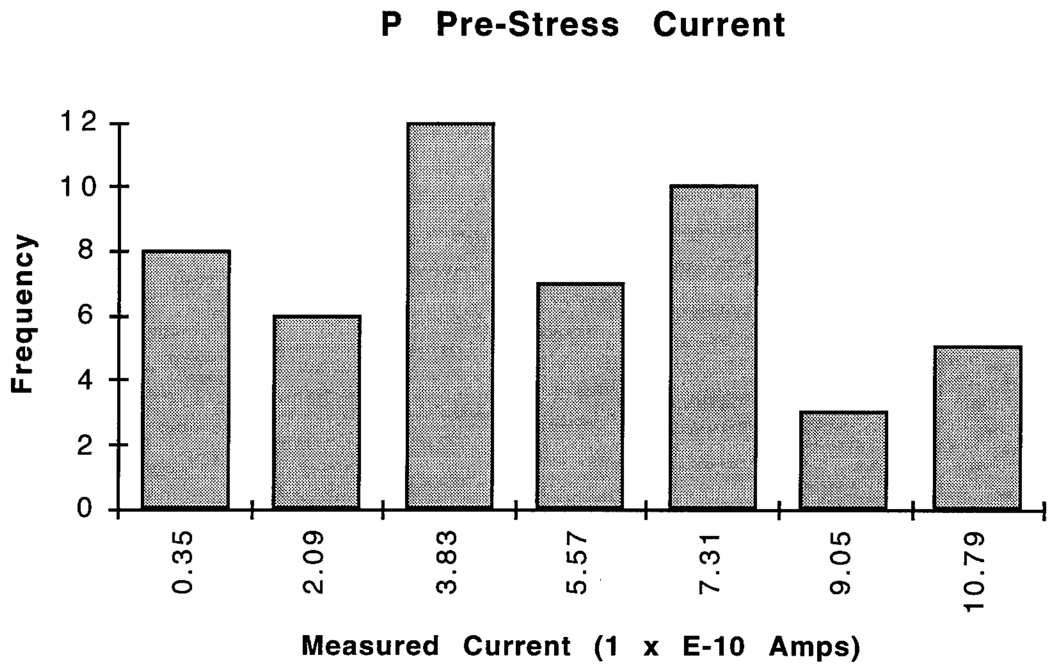

Figure 115. Uncensored Vendor B Wafer 1 P structure measured initial current.

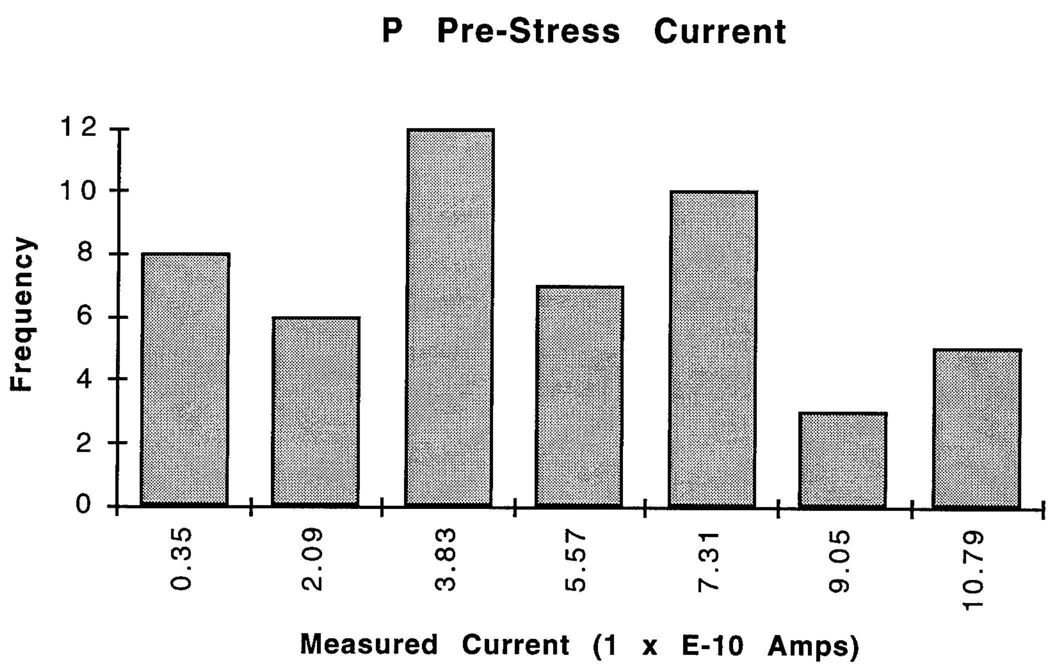

Figure 116. Censored Vendor B Wafer 1 P structure measured initial current.

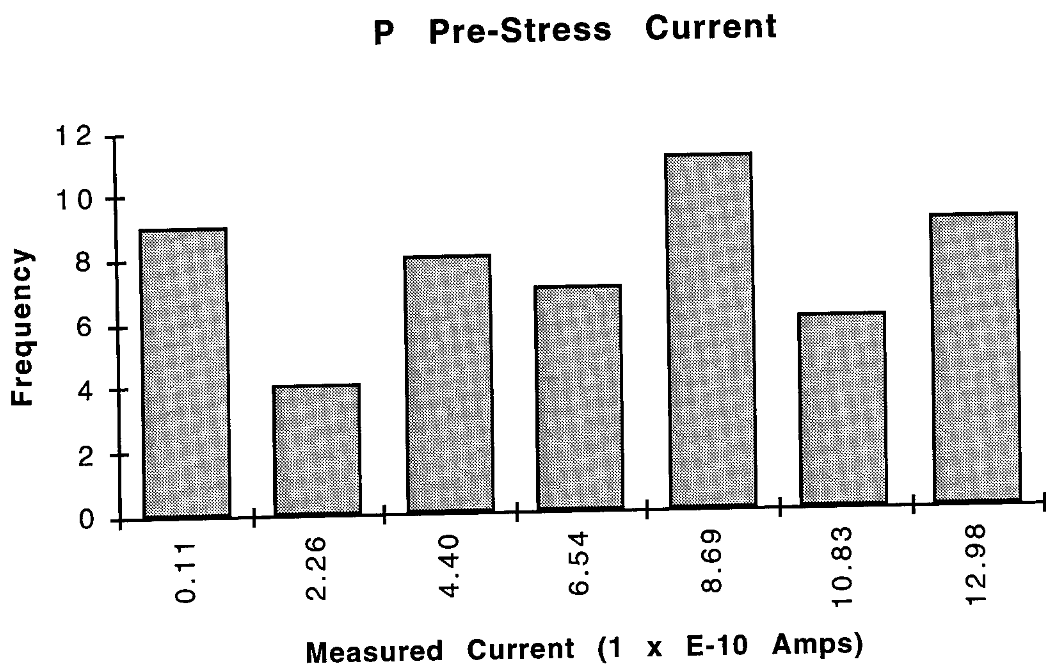

Figure 117. Uncensored Vendor B Wafer 2 P structure measured initial current.

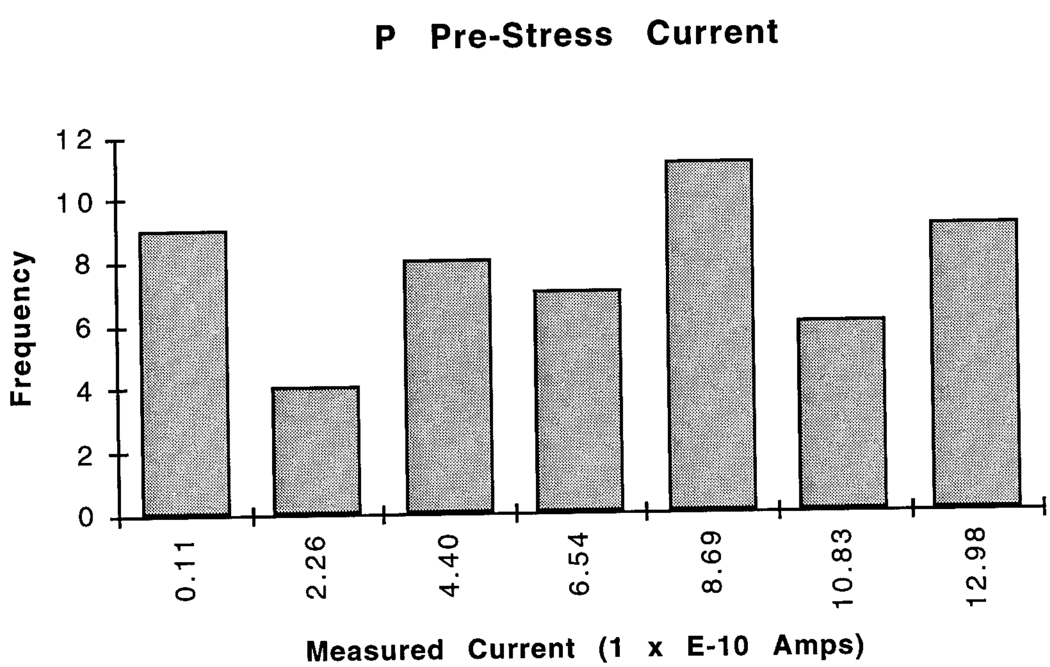

Figure 118. Censored Vendor B Wafer 2 P structure measured initial current.

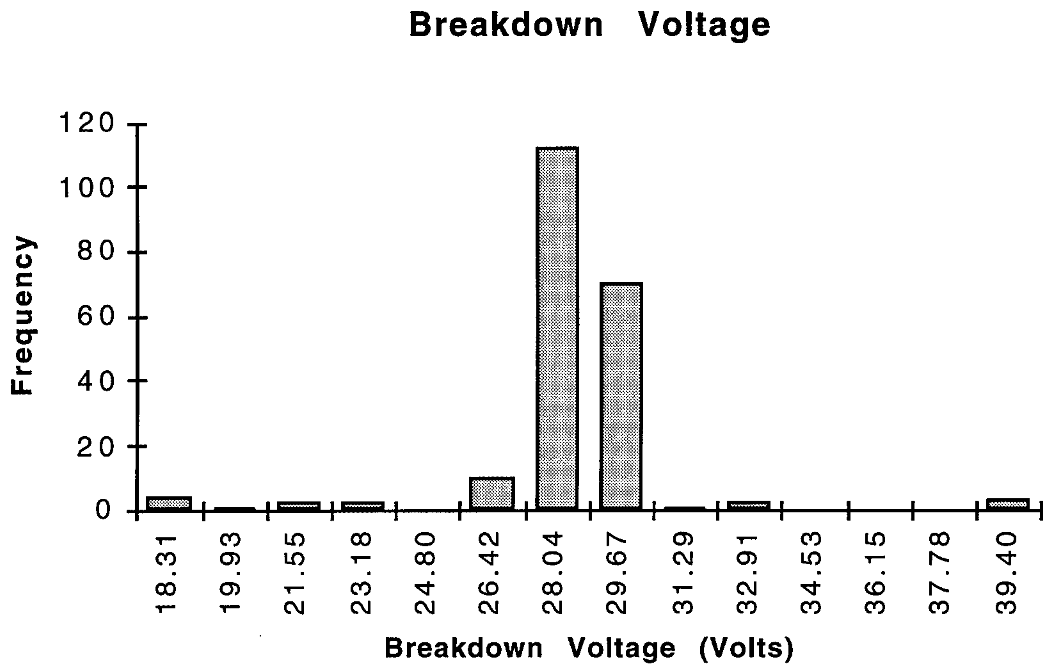

Figure 119. Uncensored Vendor B measured breakdown voltage.

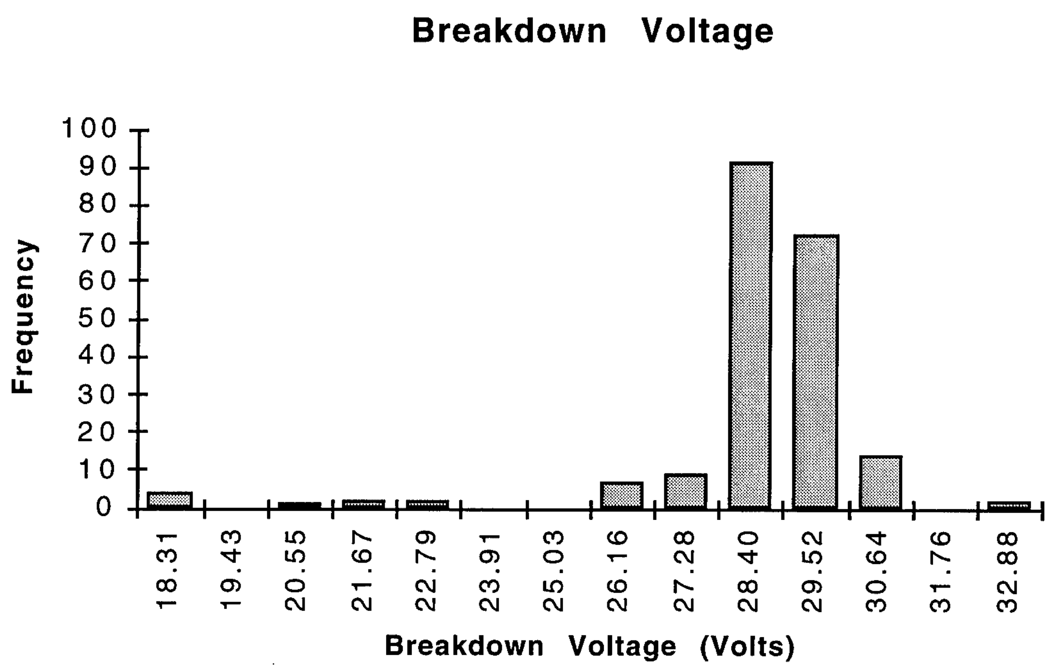

Figure 120. Censored Vendor B measured breakdown voltage.

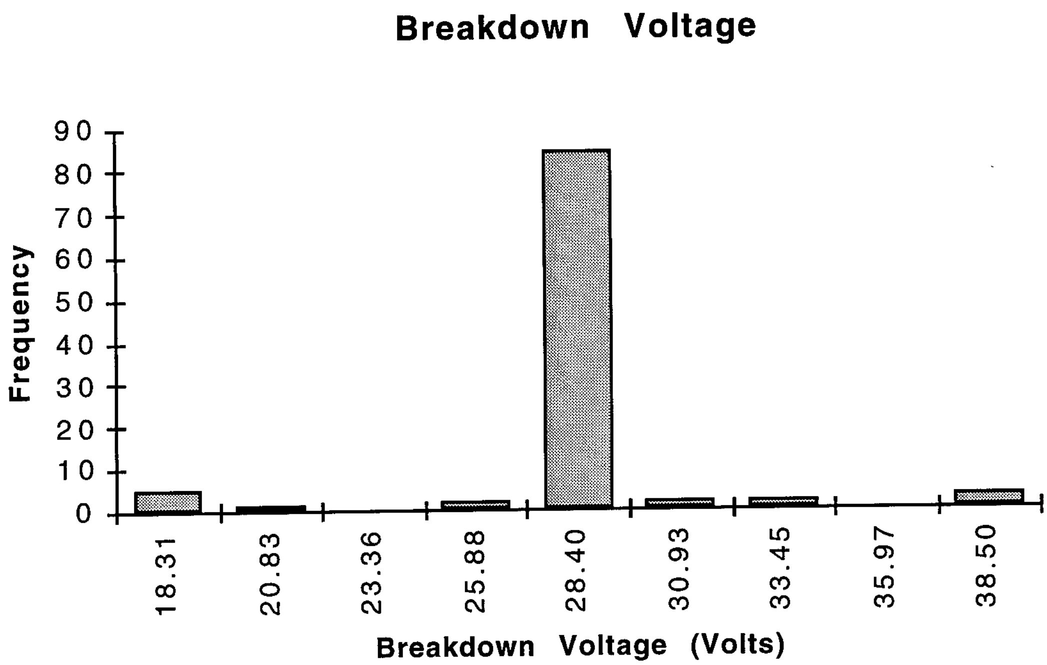

Figure 121. Uncensored Vendor B Wafer 1 measured breakdown voltage.

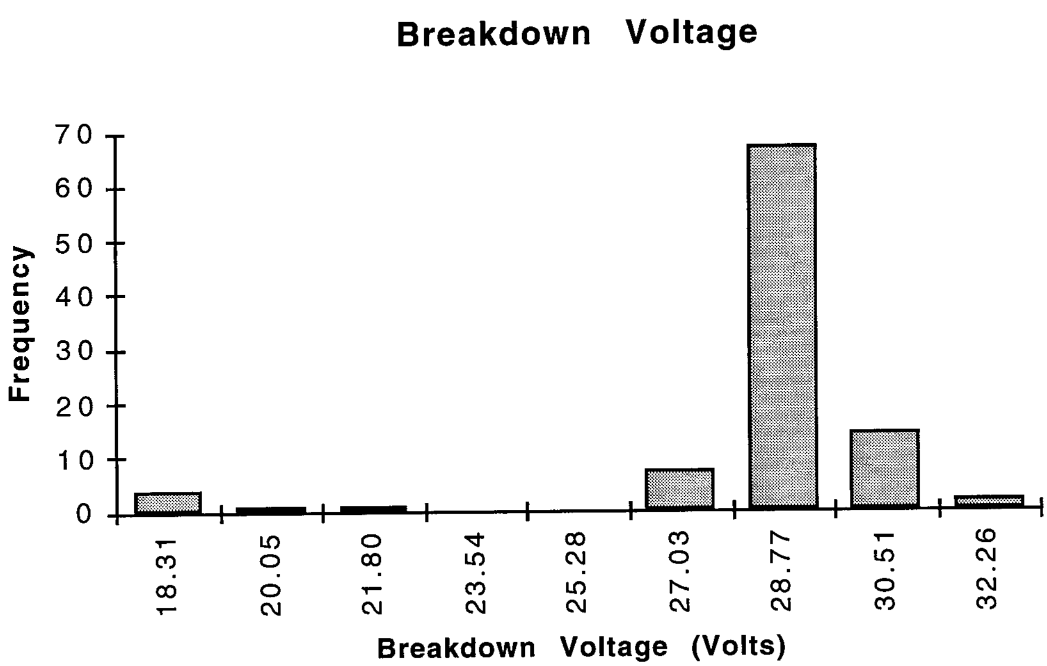

Figure 122. Censored Vendor B Wafer 1 measured breakdown voltage.

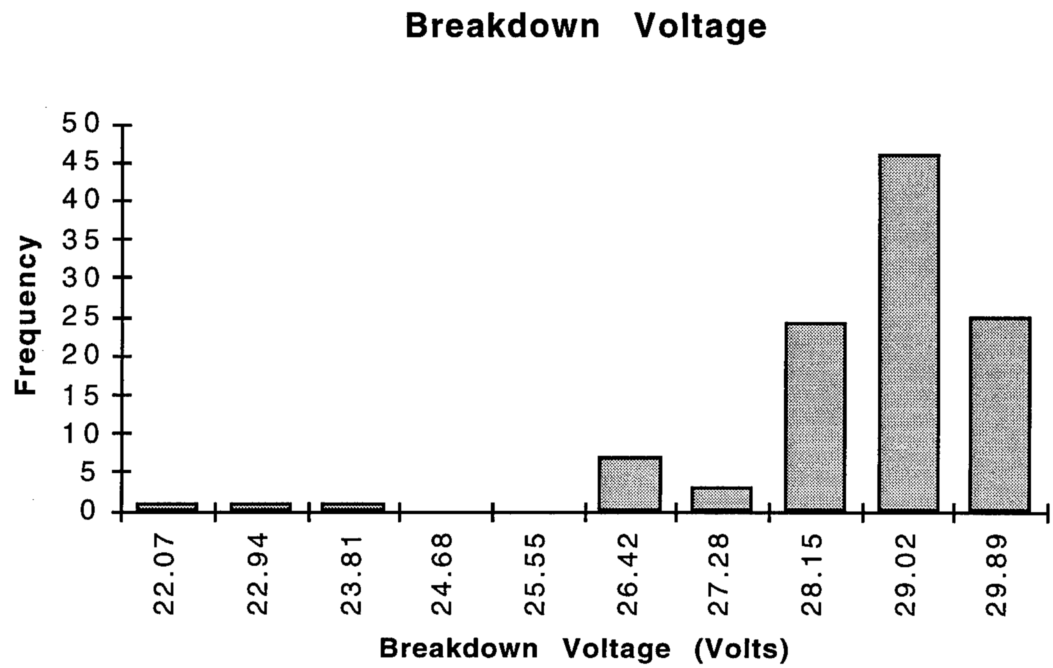

Figure 123. Uncensored Vendor B Wafer 2 measured breakdown voltage.

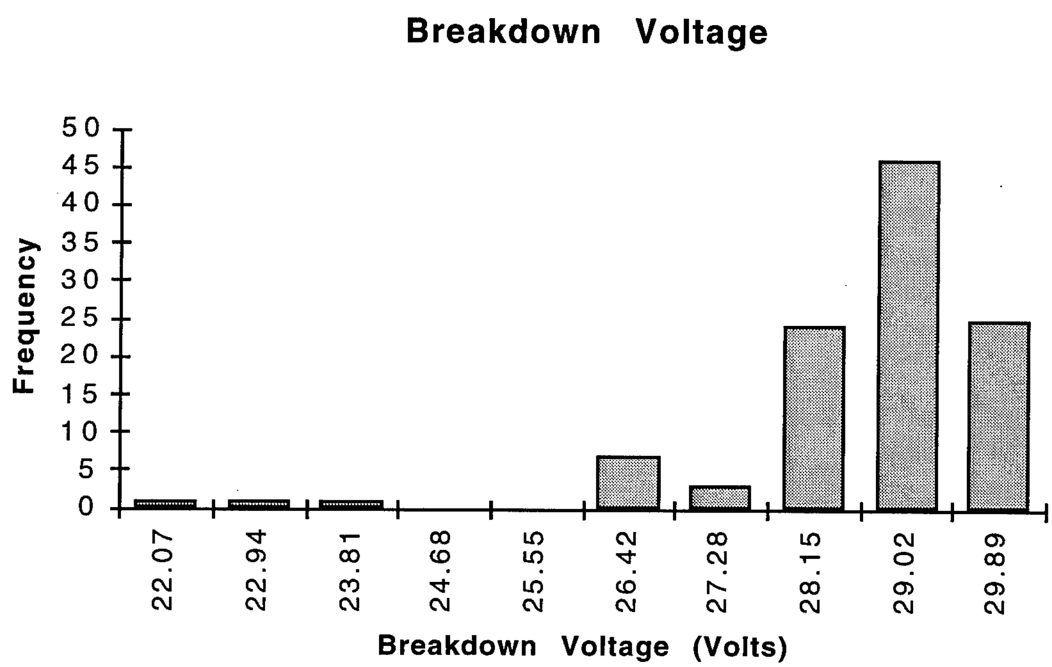

Figure 124. Censored Vendor B Wafer 2 measured breakdown voltage.

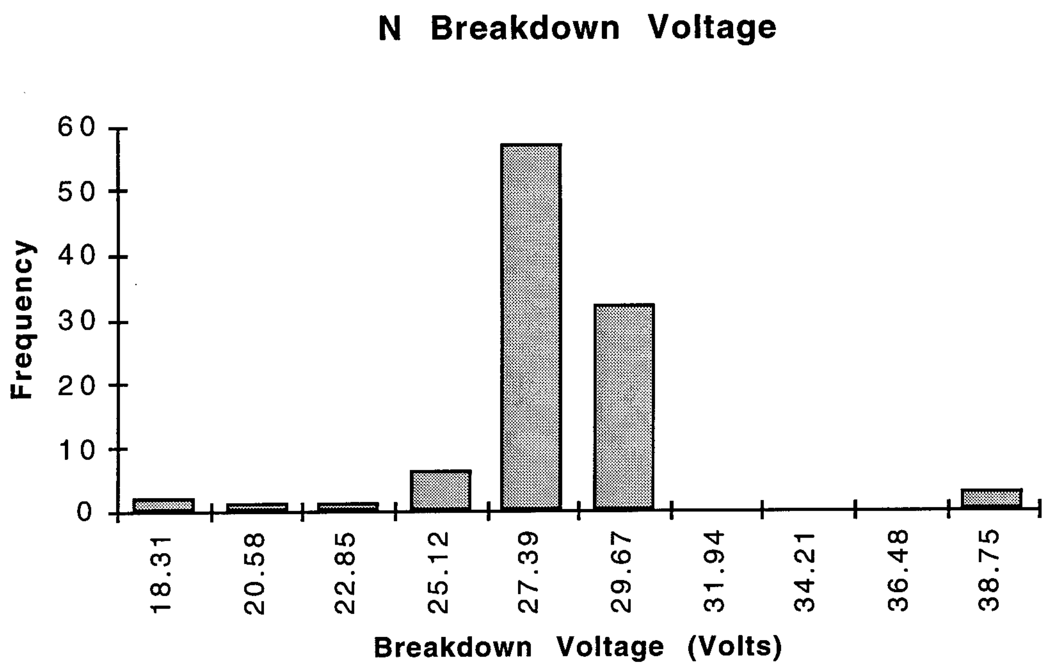

Figure 125. Uncensored Vendor B N structure measured breakdown voltage.

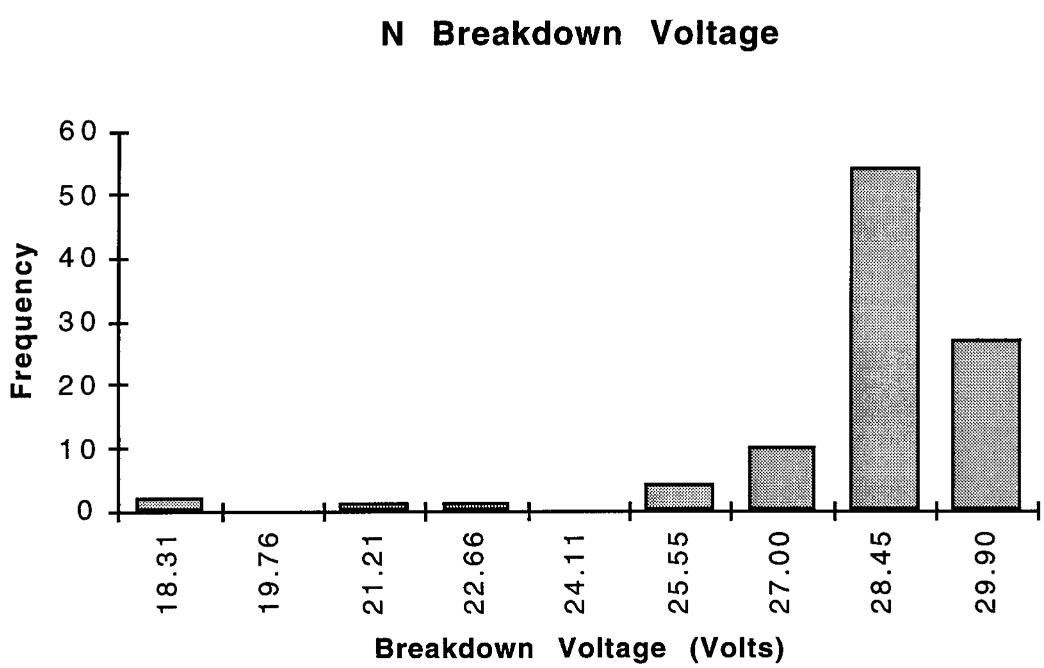

Figure 126. Censored Vendor B N structure measured breakdown voltage.

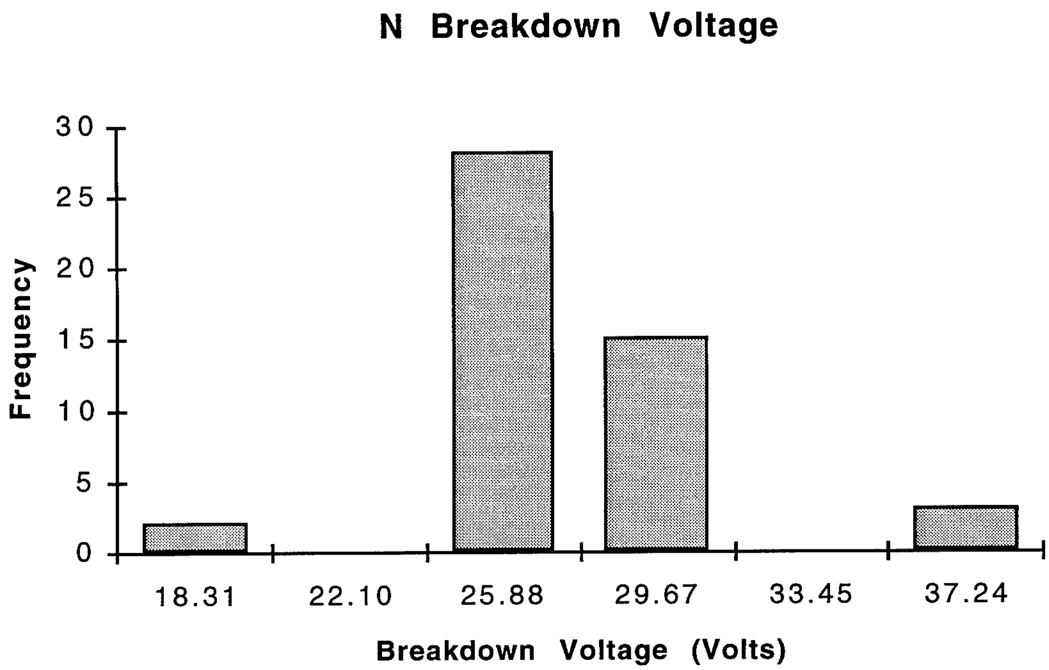

Figure 127. Uncensored Vendor B Wafer 1 N structure measured bkdn voltage.

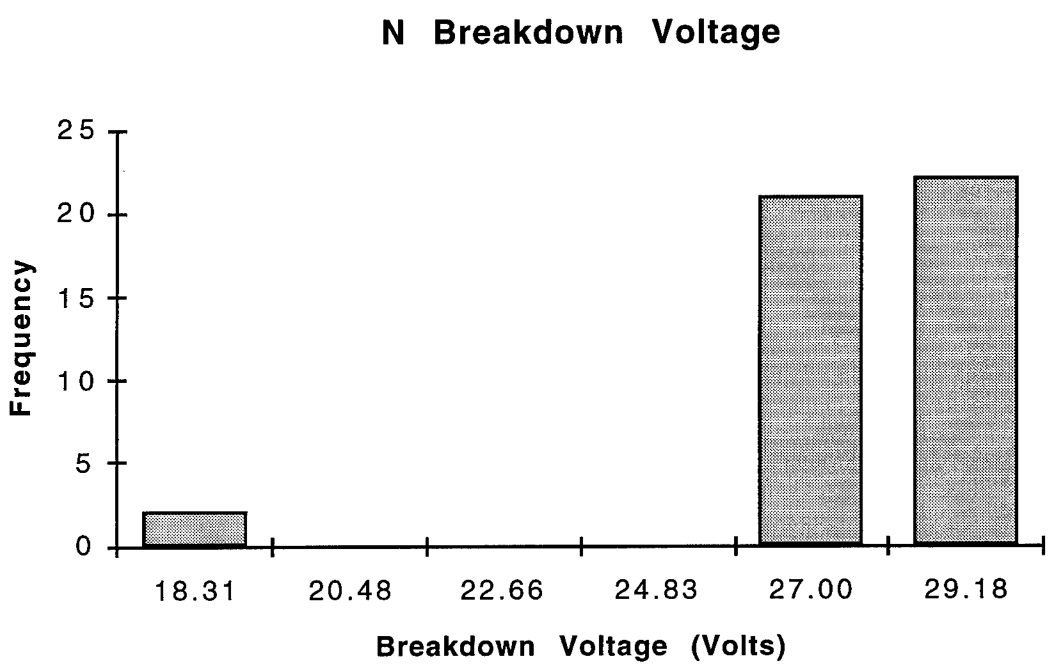

Figure 128. Censored Vendor B Wafer 1 N structure measured bkdn voltage.

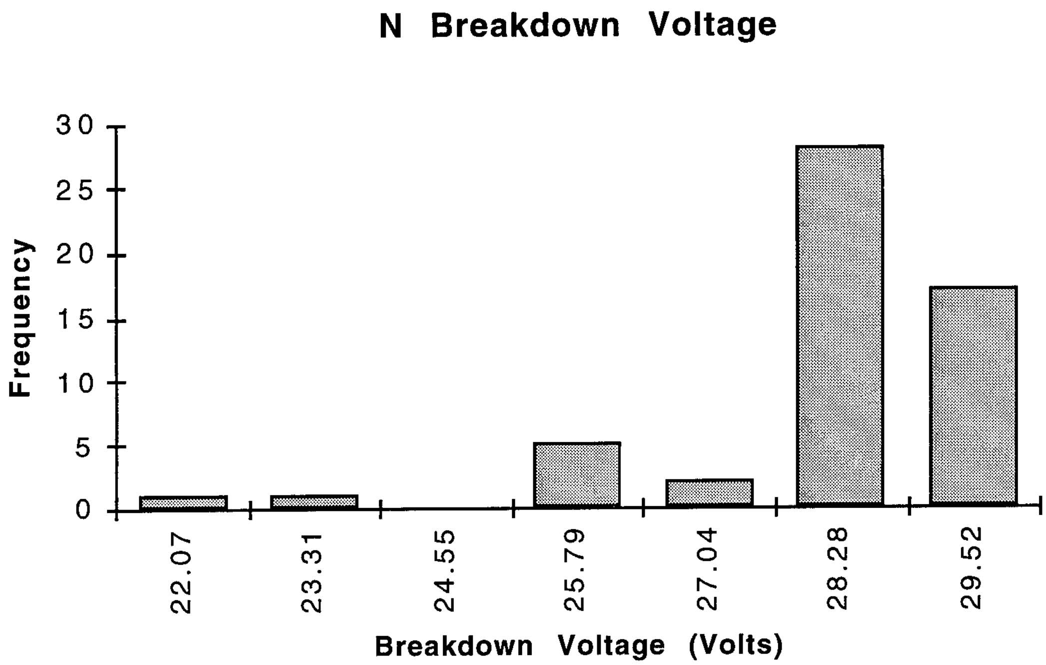

Figure 129. Uncensored Vendor B Wafer 2 N structure measured bkdn voltage.

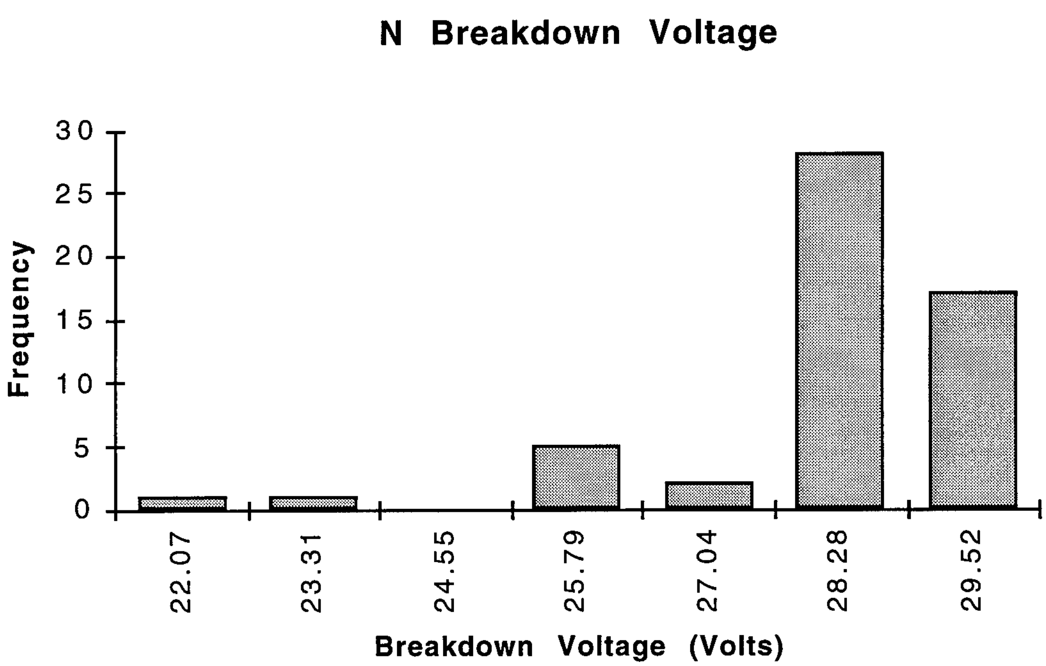

Figure 130. Censored Vendor B Wafer 2 N structure measured bkdn voltage.

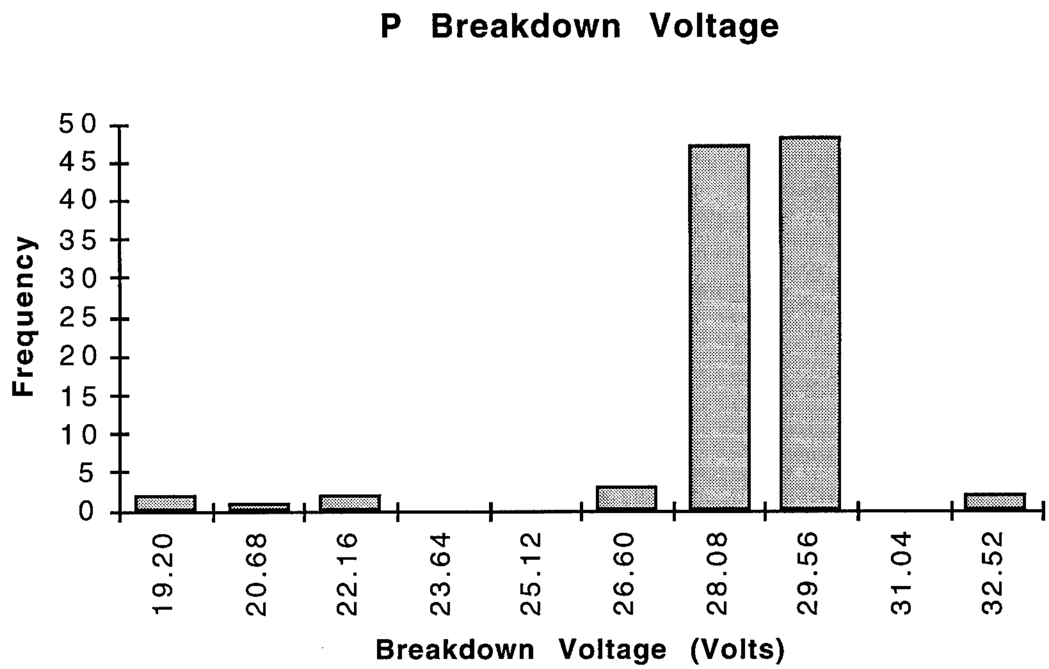

Figure 131. Uncensored Vendor B P structure measured breakdown voltage.

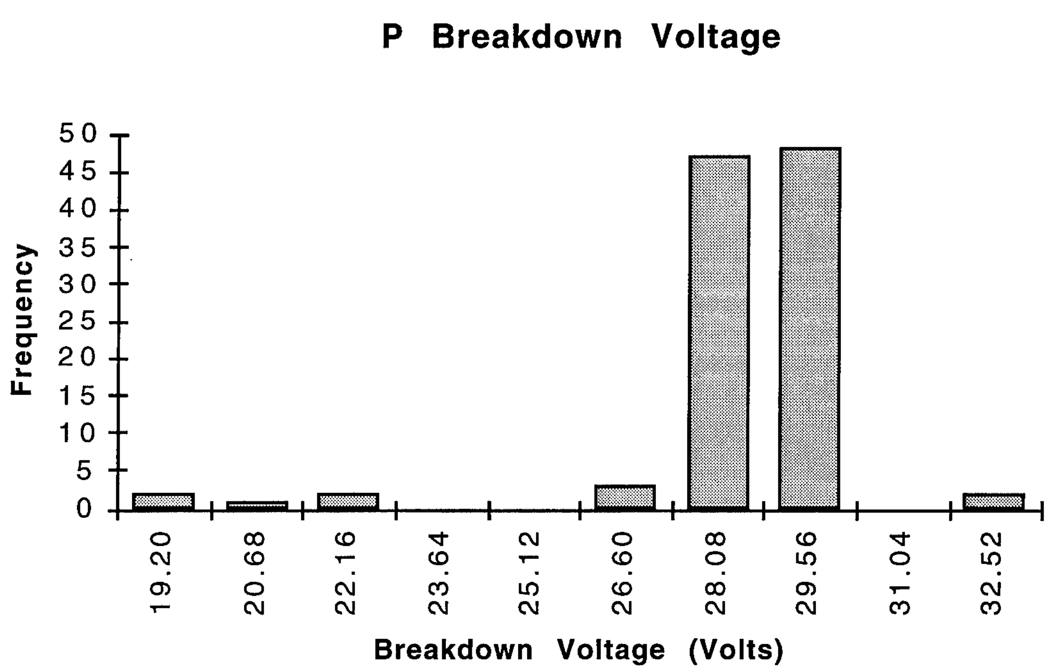

Figure 132. Censored Vendor B P structure measured breakdown voltage.

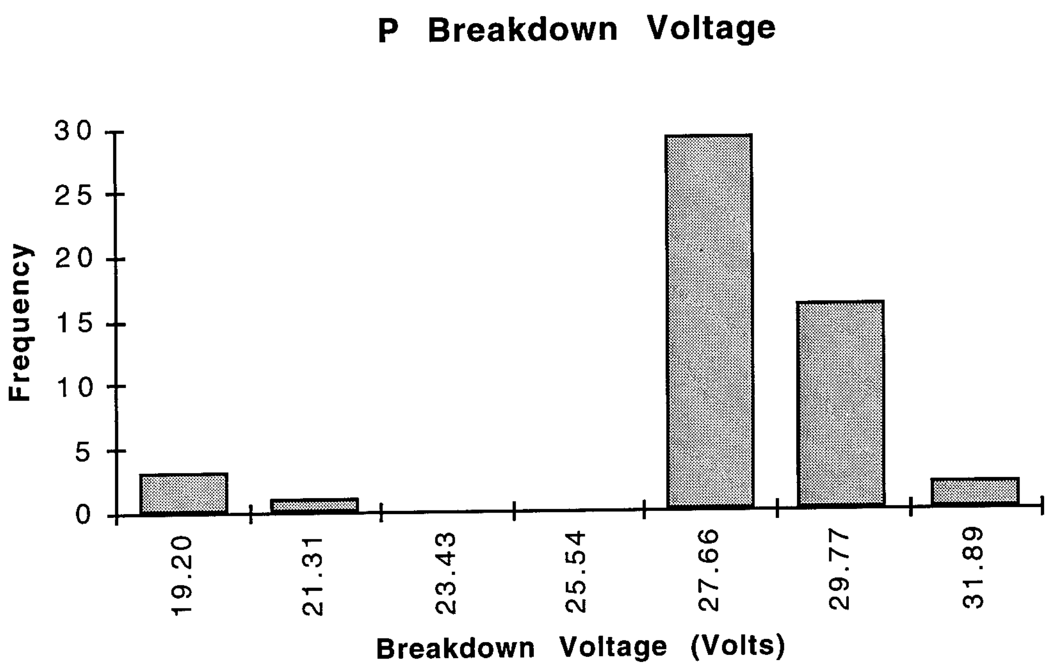

Figure 133. Uncensored Vendor B Wafer 1 P structure measured bkdn voltage.

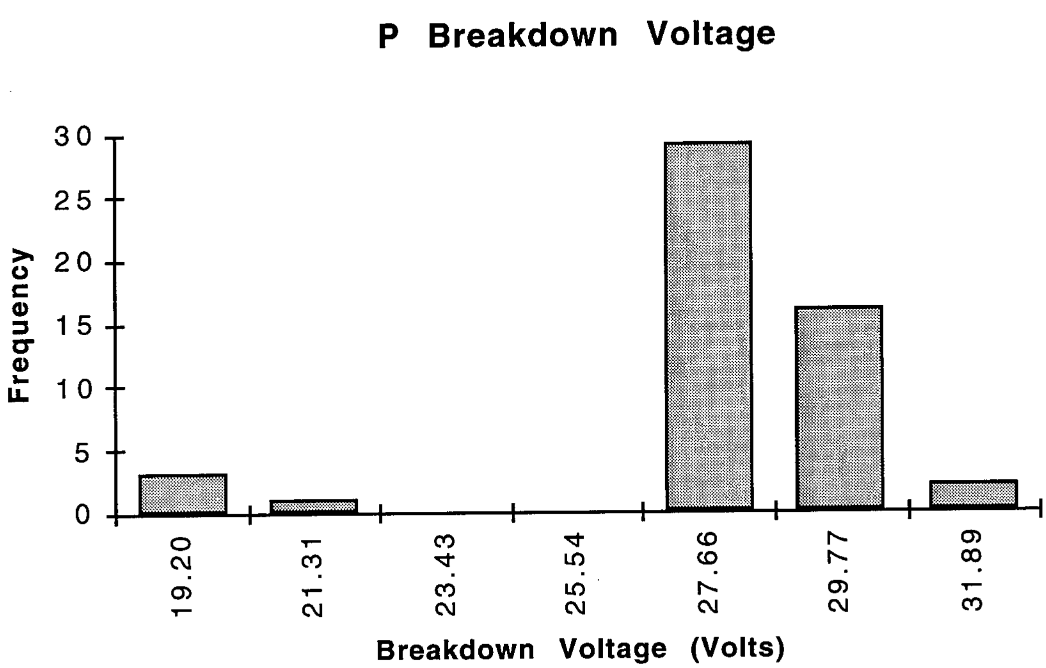

Figure 134. Censored Vendor B Wafer 1 P structure measured bkdn voltage.

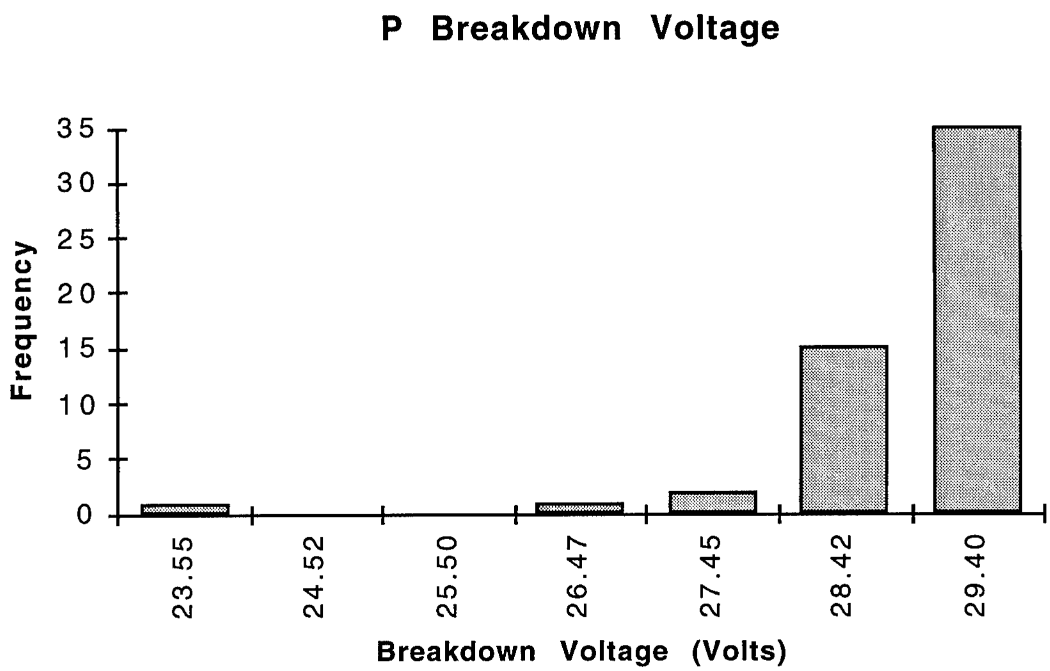

Figure 135. Uncensored Vendor B Wafer 2 P structure measured bkdn voltage.

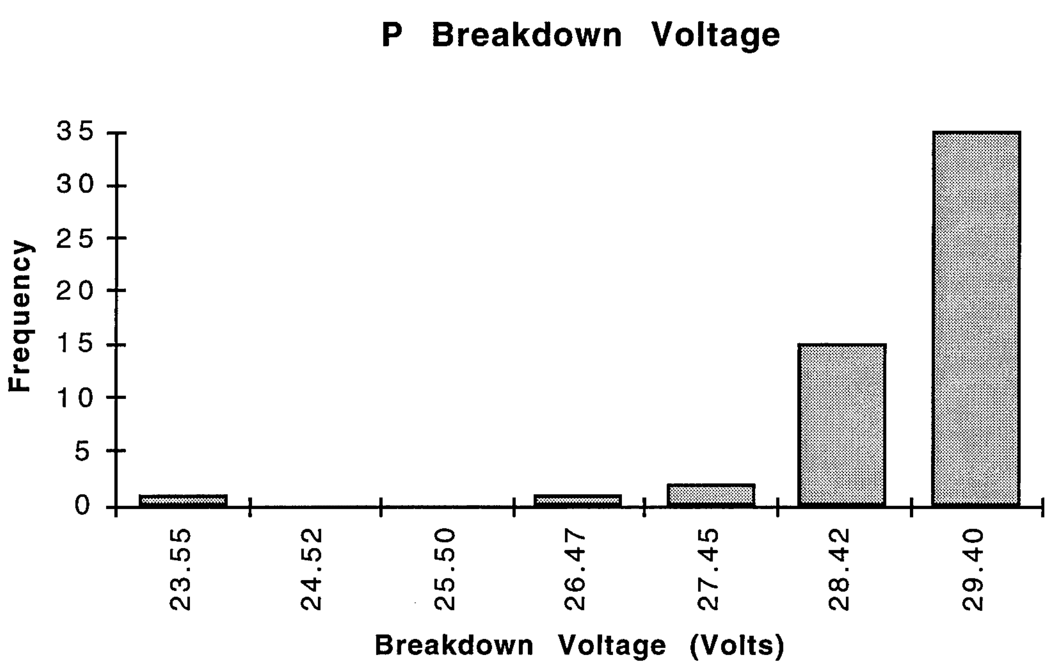

Figure 136. Censored Vendor B Wafer 2 P structure measured bkdn voltage.

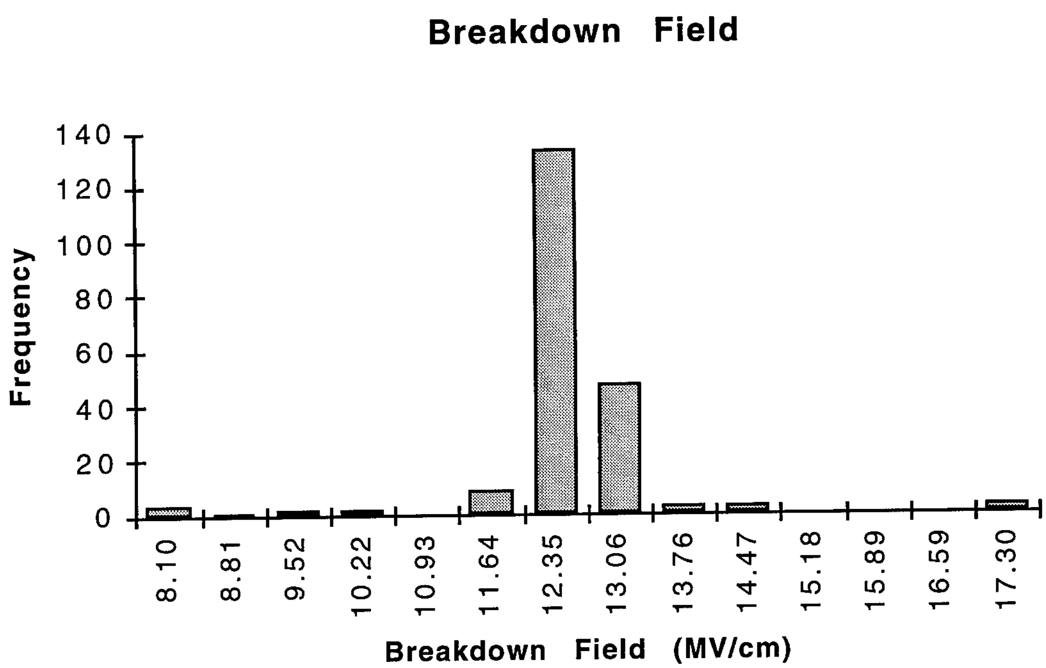

Figure 137. Uncensored Vendor B calculated breakdown field.

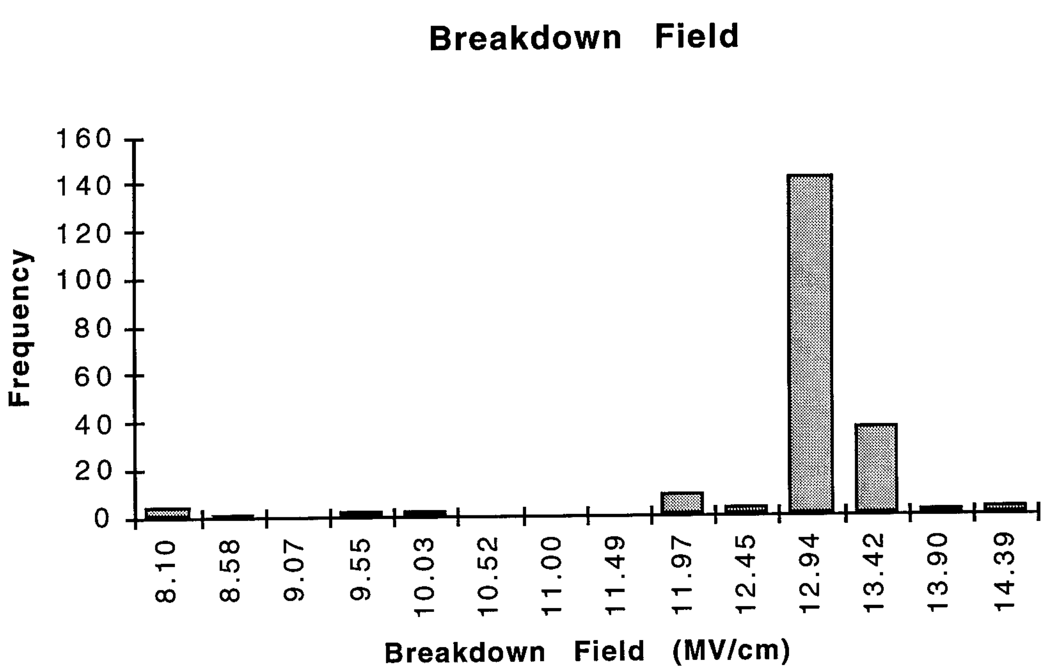

Figure 138. Censored Vendor B calculated breakdown field.

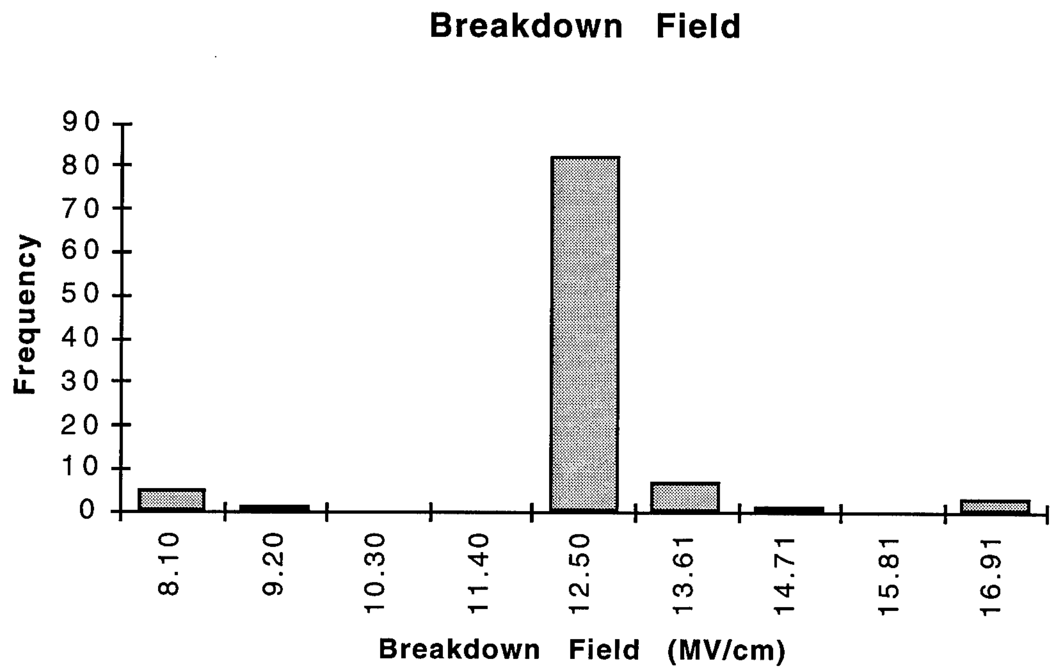

Figure 139. Uncensored Vendor B Wafer 1 calculated breakdown field.

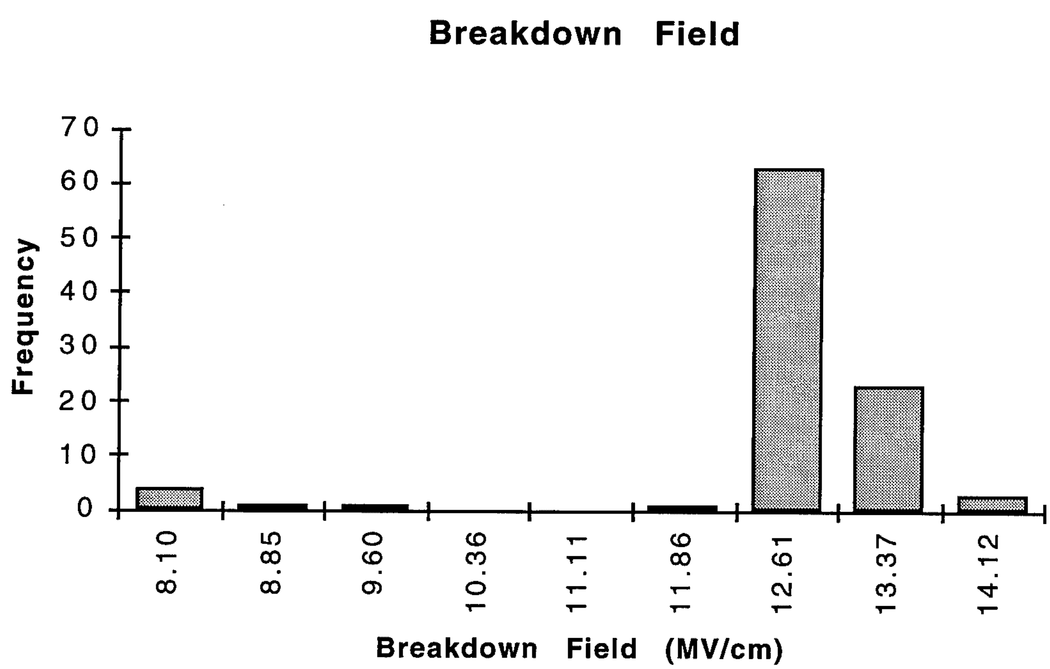

Figure 140. Censored Vendor B Wafer 1 calculated breakdown field.

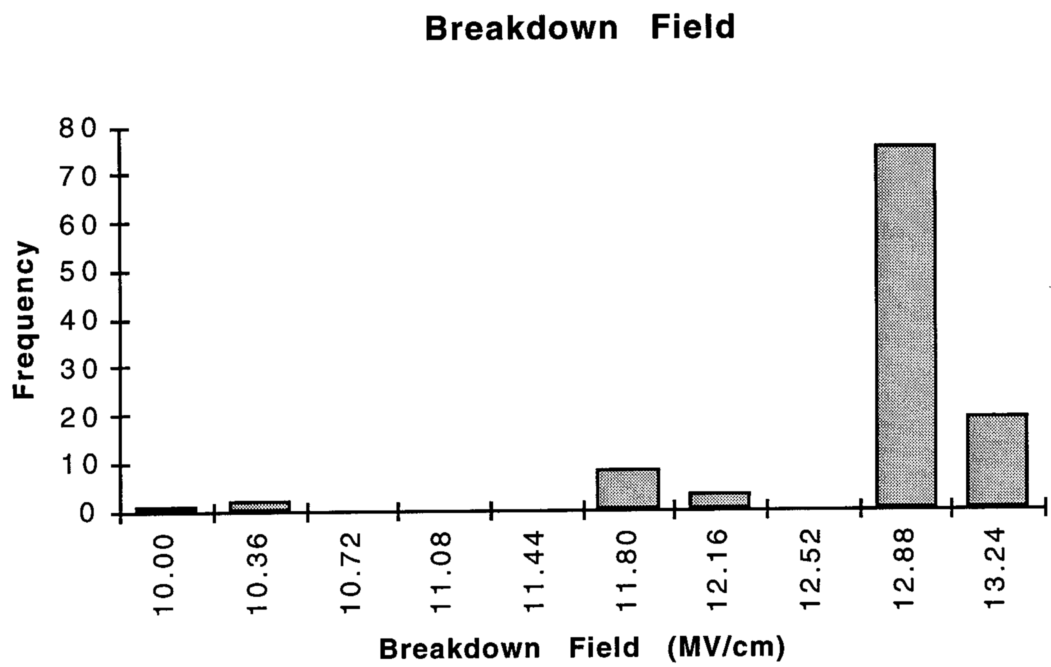

Figure 141. Uncensored Vendor B Wafer 2 calculated breakdown field.

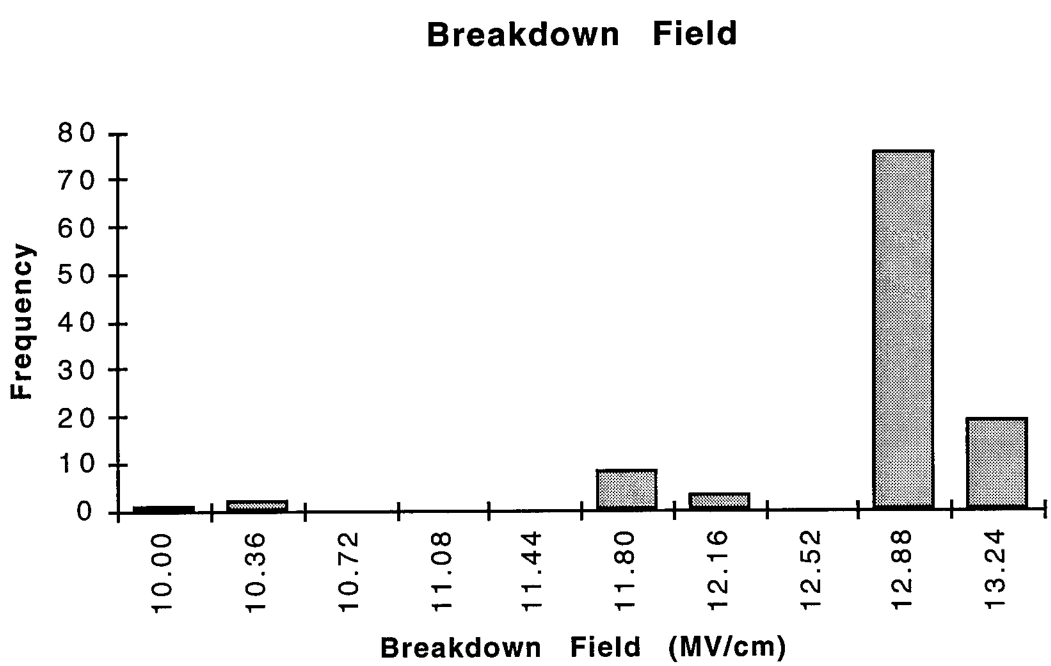

Figure 142. Censored Vendor B Wafer 2 calculated breakdown field.

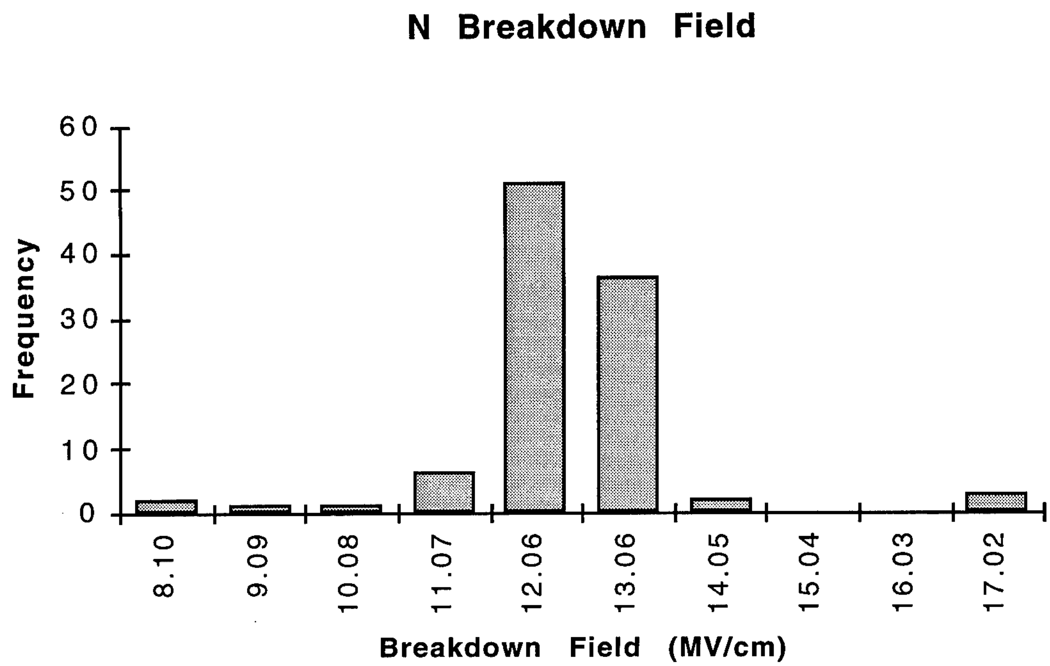

Figure 143. Uncensored Vendor B N structure calculated breakdown field.

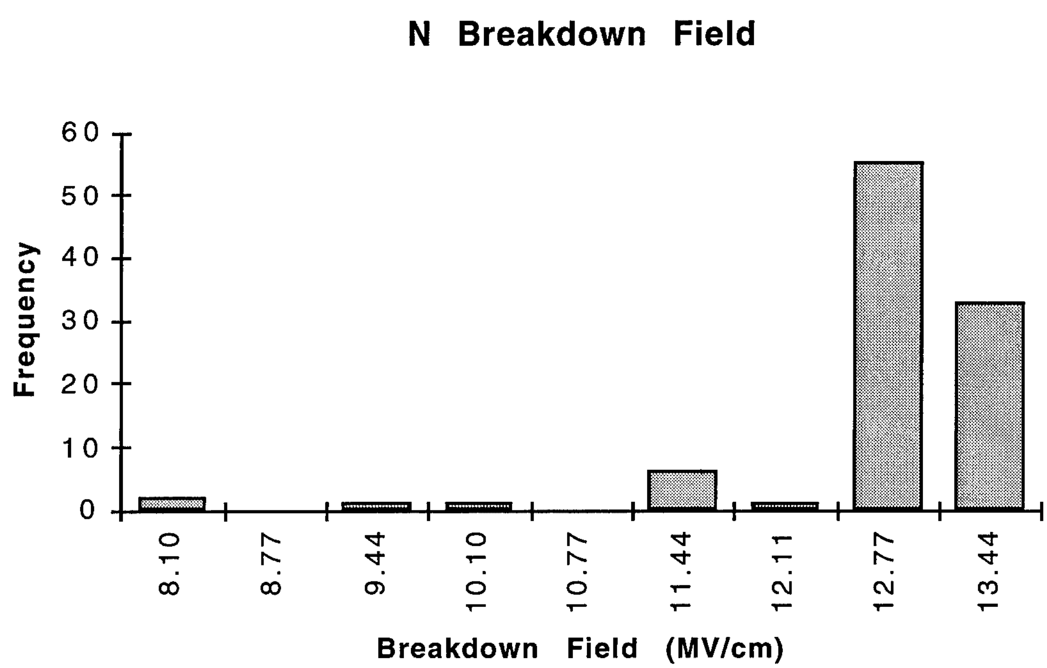

Figure 144. Censored Vendor B N structure calculated breakdown field.

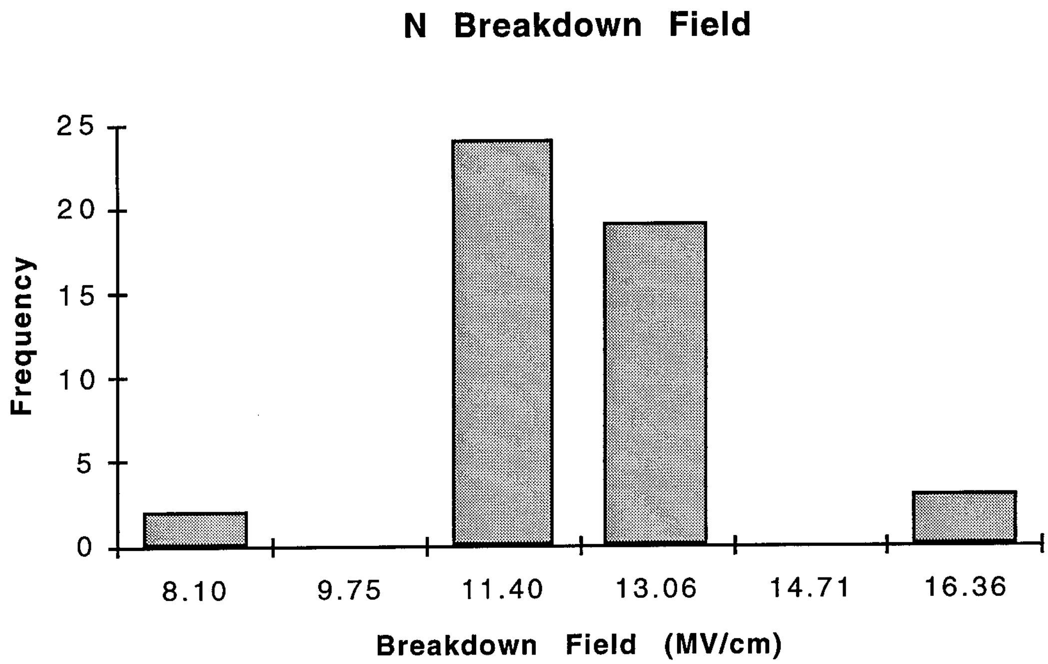

Figure 145. Uncensored Vendor B Wafer 1 N structure calculated bkdn field.

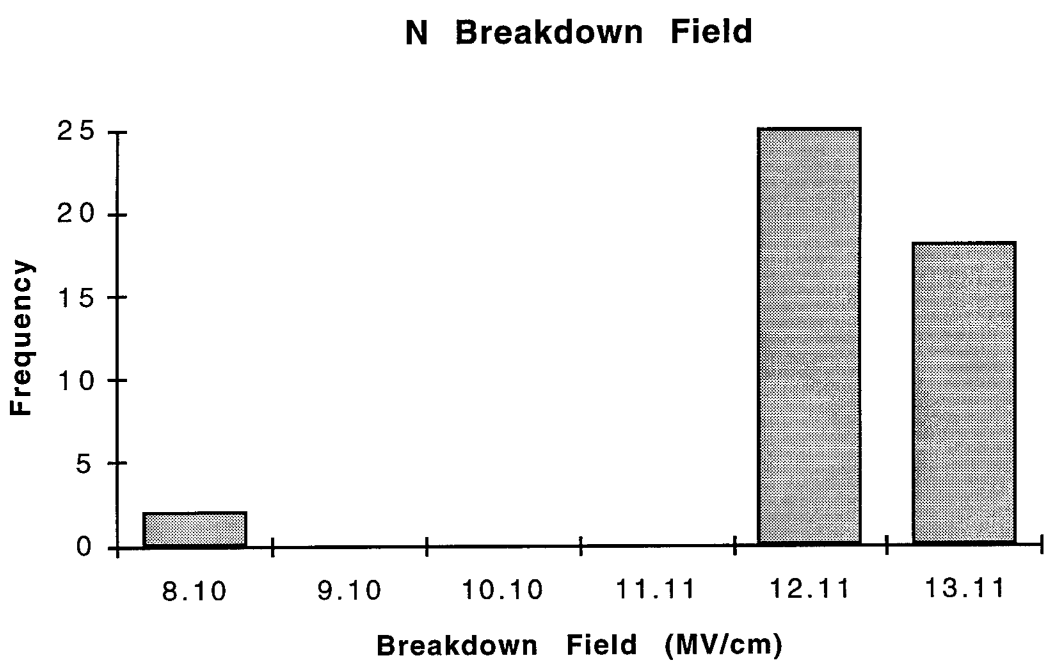

Figure 146. Censored Vendor B Wafer 1 N structure calculated breakdown field.

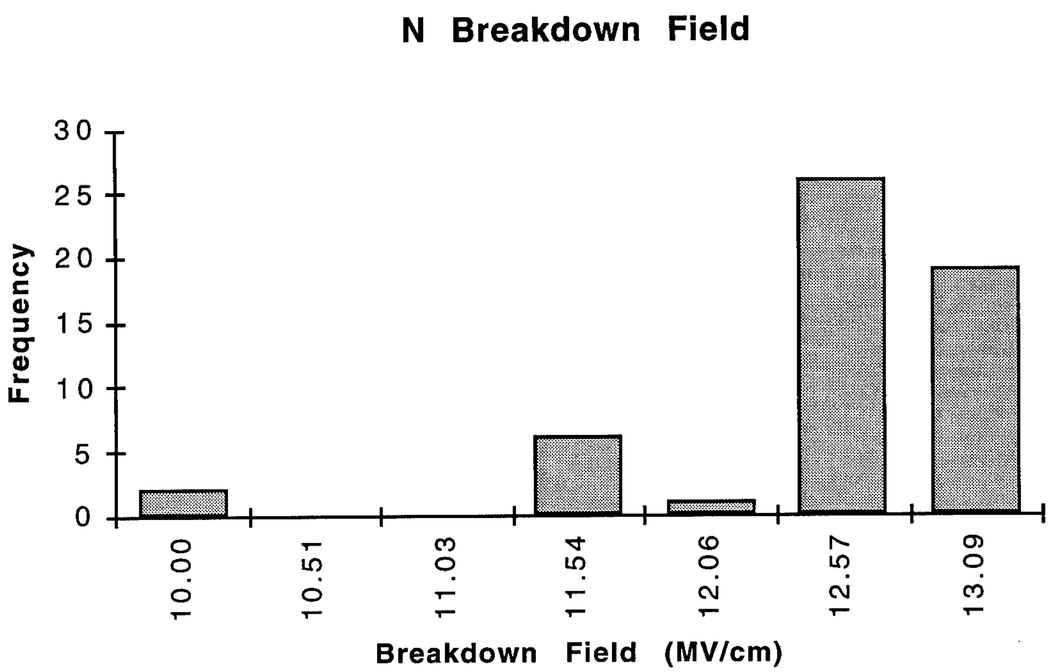

Figure 147. Uncensored Vendor B Wafer 2 N structure calculated bkdn field.

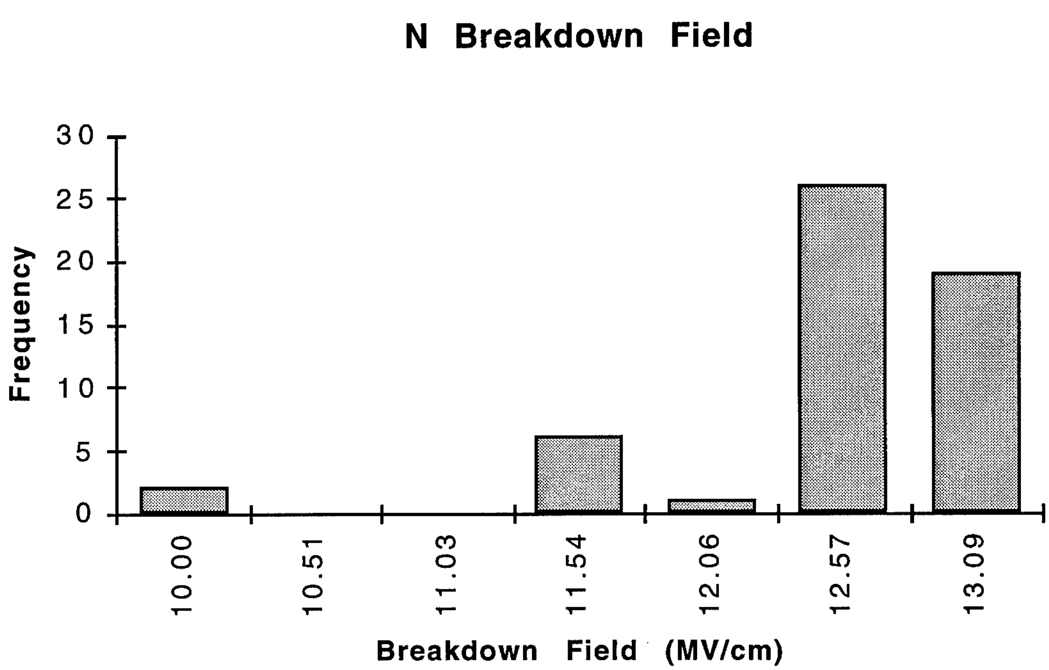

Figure 148. Censored Vendor B Wafer 2 N structure calculated breakdown field.

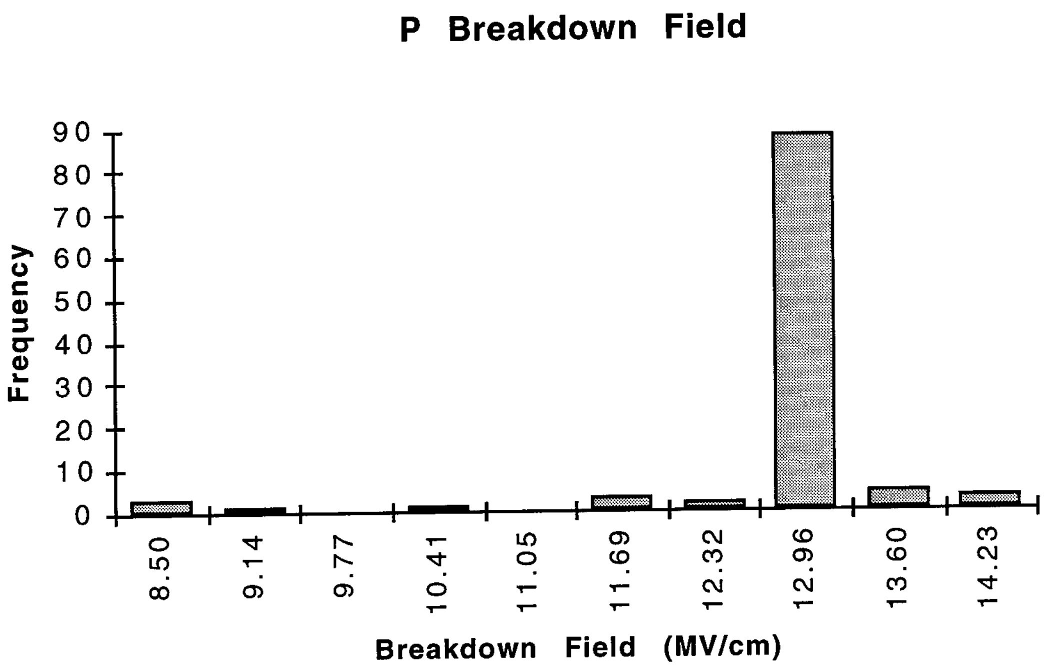

Figure 149. Uncensored Vendor B P structure calculated breakdown field.

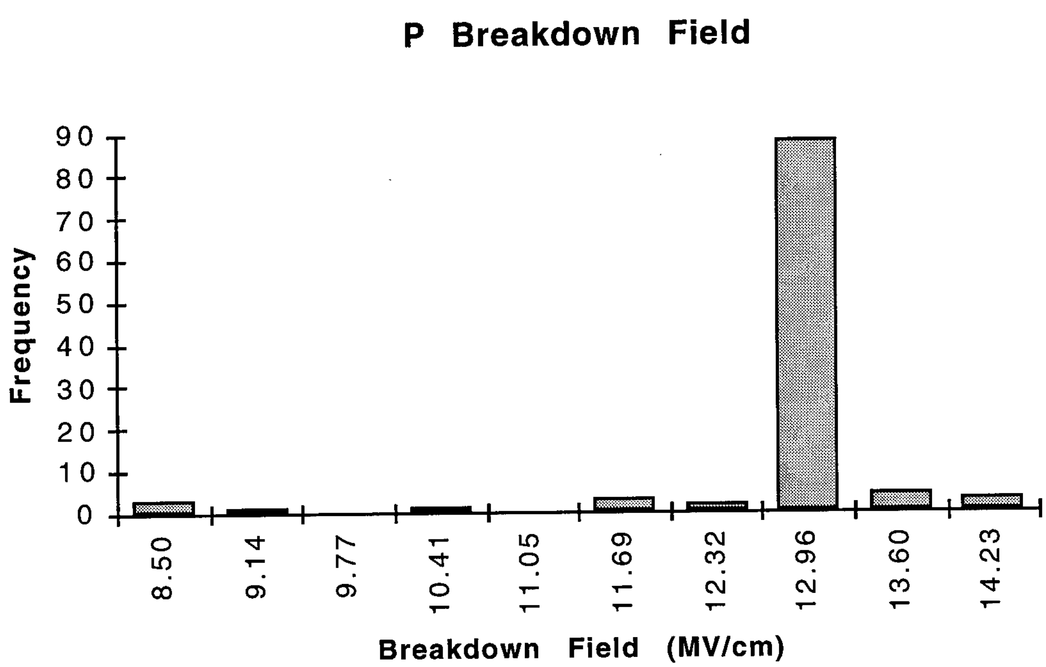

Figure 150. Censored Vendor B P structure calculated breakdown field.

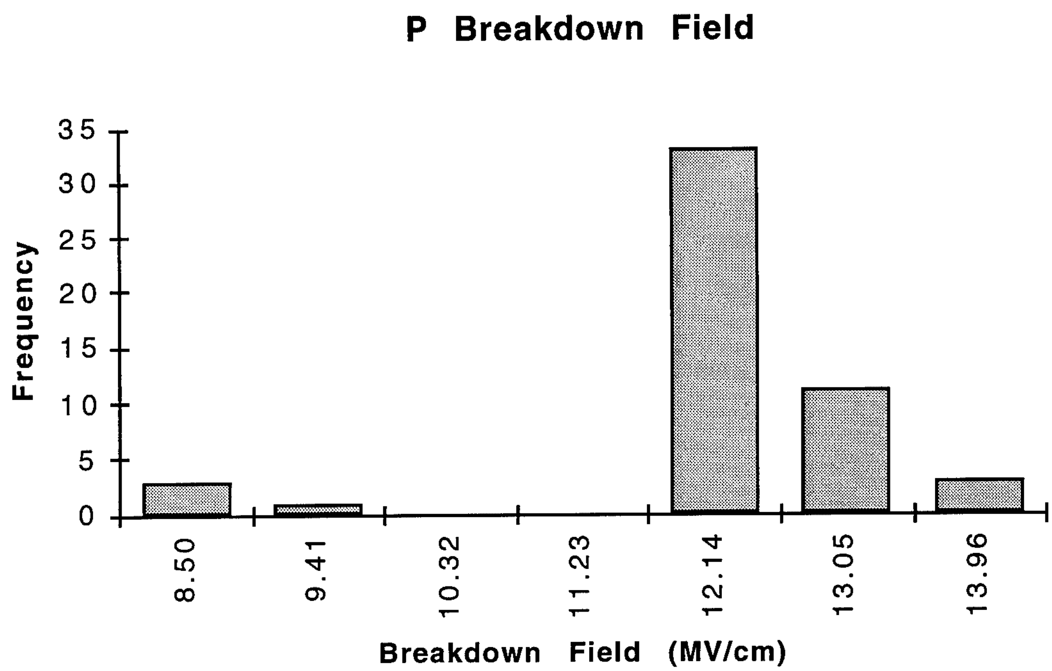

Figure 151. Uncensored Vendor B Wafer 1 P structure calculated bkdn field.

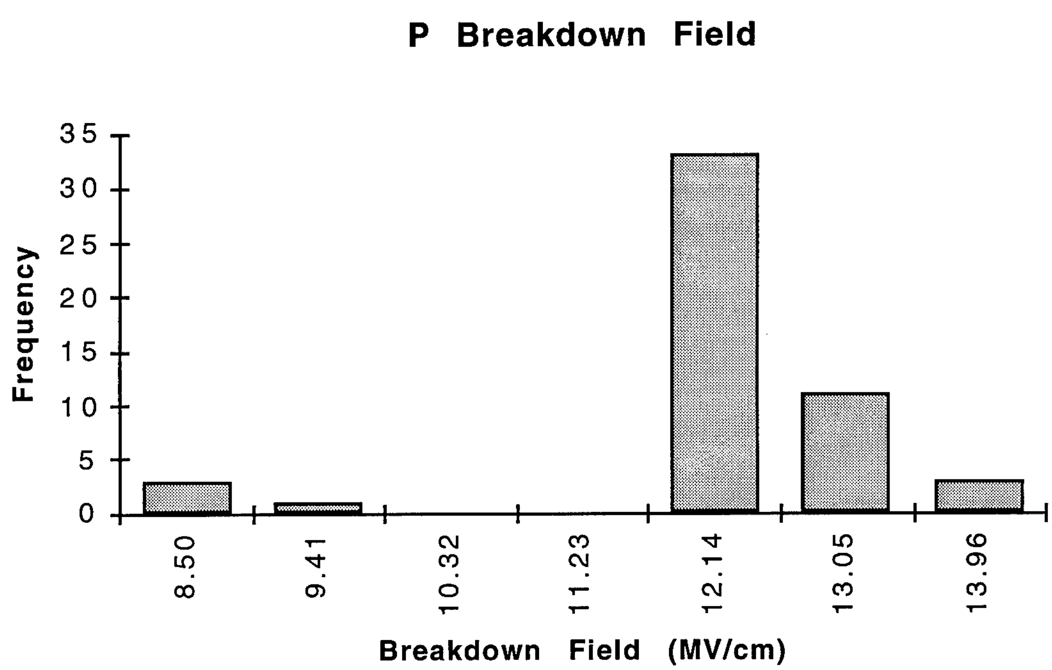

Figure 152. Censored Vendor B Wafer 1 P structure calculated breakdown field.

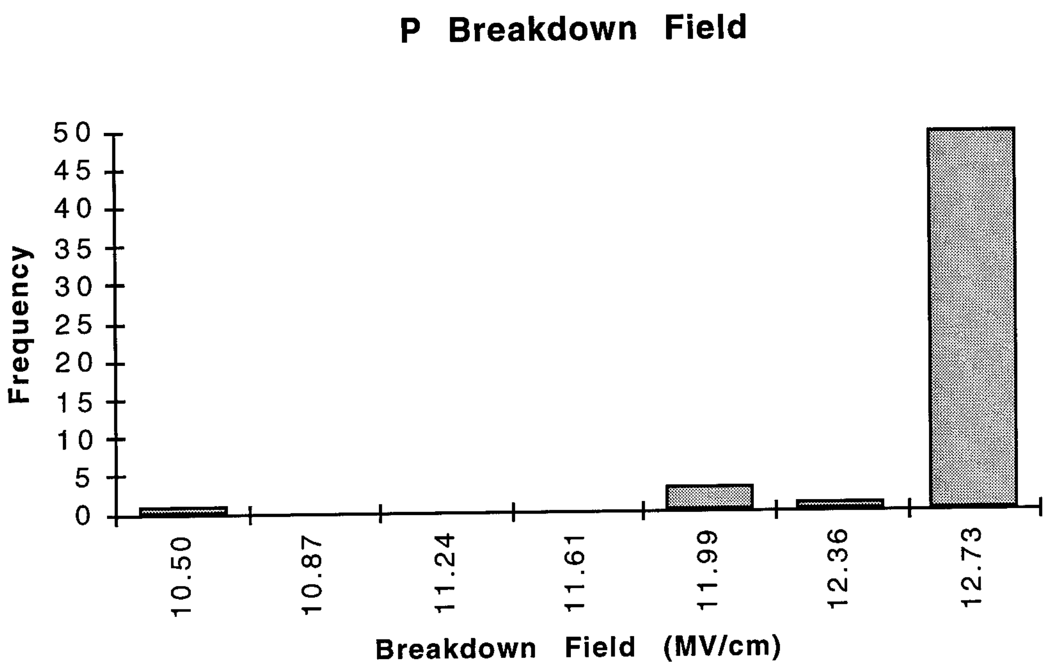

Figure 153. Uncensored Vendor B wafer 2 P structure calculated bkdn field.

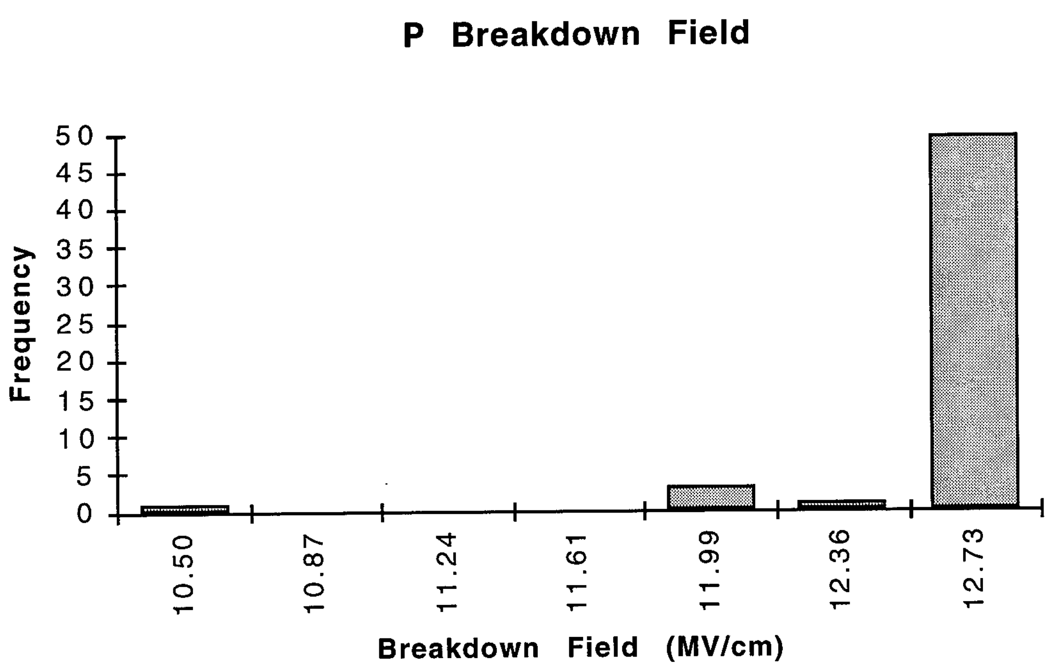

Figure 154. Censored Vendor B Wafer 2 P structure calculated breakdown field.

APPENDIX F: CUMULATIVE BREAKDOWN DATA

Table 49. Uncensored Vendor A Raw Breakdown Data.

	Field																		
	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
0.1	0	0	0	0	0	0	0	9	4	10	12	0	0	0	0	0	0	0	0
0.3	0	0	0	0	0	0	0	0	0	9	2	0	0	0	0	0	0	0	0
0.5	0	0	0	0	0	0	0	0	0	5	13	0	0	0	0	0	0	0	0
0.7	0	0	0	0	0	0	0	0	0	6	3	1	0	0	0	0	0	0	0
1.0	1	0	0	0	0	0	0	0	0	6	11	0	0	0	0	0	0	0	1
N 0.1	0	0	0	0	0	0	0	4	2	6	6	0	0	0	0	0	0	0	0
N 0.3	0	0	0	0	0	0	0	0	0	3	1	0	0	0	0	0	0	0	0
N 0.5	0	0	0	0	0	0	0	0	0	3	8	0	0	0	0	0	0	0	0
N 0.7	0	0	0	0	0	0	0	0	0	4	1	0	0	0	0	0	0	0	0
N 1.0	1	0	0	0	0	0	0	0	0	2	5	0	0	0	0	0	0	0	0
N	1	0	0	0	0	0	0	4	2	18	21	0	0	0	0	0	0	0	0
P 0.1	0	0	0	0	0	0	0	5	2	4	6	0	0	0	0	0	0	0	0
P 0.3	0	0	0	0	0	0	0	0	0	6	1	0	0	0	0	0	0	0	0
P 0.5	0	0	0	0	0	0	0	0	0	2	5	0	0	0	0	0	0	0	0
P 0.7	0	0	0	0	0	0	0	0	0	2	2	1	0	0	0	0	0	0	0
P 1.0	0	0	0	0	0	0	0	0	0	4	6	0	0	0	0	0	0	0	1
P	0	0	0	0	0	0	0	5	2	18	20	1	0	0	0	0	0	0	1
Total	1	0	0	0	0	0	0	9	4	36	41	1	0	0	0	0	0	0	1

Table 50. Uncensored Vendor A Cumulative Breakdown Data.

	Field																		
	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22
0.1	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.26	0.37	0.66	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
0.3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.82	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
0.5	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.28	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
0.7	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.60	0.90	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
1.0	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.05	0.37	0.95	0.95	0.95	0.95	0.95	0.95	0.95	0.95	1.00
N 0.1	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.22	0.33	0.67	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
N 0.3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.75	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
N 0.5	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.27	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
N 0.7	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.80	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
N 1.0	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.13	0.38	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
N	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.11	0.15	0.54	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
P 0.1	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.29	0.41	0.65	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
P 0.3	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.86	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
P 0.5	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.29	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
P 0.7	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.40	0.80	1.00	1.00	1.00	1.00	1.00	1.00	1.00	1.00
P 1.0	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.36	0.91	0.91	0.91	0.91	0.91	0.91	0.91	0.91	1.00
P	0.00	0.00	0.00	0.00	0.00	0.00	0.00	0.11	0.15	0.53	0.96	0.98	0.98	0.98	0.98	0.98	0.98	0.98	1.00
Total	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.11	0.15	0.54	0.98	0.99	0.99	0.99	0.99	0.99	0.99	0.99	1.00

Table 51. Censored Vendor A Raw Breakdown Data.

	Field				
	11	12	13	14	15
0.1	9	4	10	12	0
0.3	0	0	9	2	0
0.5	0	0	5	13	0
0.7	0	0	6	3	1
1	0	0	6	11	0
N 0.1	4	2	6	6	0
N 0.3	0	0	3	1	0
N 0.5	0	0	3	8	0
N 0.7	0	0	4	1	0
N 1.0	0	0	2	5	0
N	4	2	18	21	0
P 0.1	5	2	4	6	0
P 0.3	0	0	6	1	0
P 0.5	0	0	2	5	0
P 0.7	0	0	2	2	1
P 1.0	0	0	4	6	0
P	5	2	18	20	1
Total	9	4	36	41	1

Table 52. Censored Vendor A Cumulative Breakdown Data.

	Field				
	11	12	13	14	15
0.1	0.26	0.37	0.66	1.00	1.00
0.3	0.00	0.00	0.82	1.00	1.00
0.5	0.00	0.00	0.28	1.00	1.00
0.7	0.00	0.00	0.60	0.90	1.00
1	0.00	0.00	0.35	1.00	1.00
N 0.1	0.22	0.33	0.67	1.00	1.00
N 0.3	0.00	0.00	0.75	1.00	1.00
N 0.5	0.00	0.00	0.27	1.00	1.00
N 0.7	0.00	0.00	0.80	1.00	1.00
N 1.0	0.00	0.00	0.29	1.00	1.00
N	0.09	0.13	0.53	1.00	1.00
P 0.1	0.29	0.41	0.65	1.00	1.00
P 0.3	0.00	0.00	0.86	1.00	1.00
P 0.5	0.00	0.00	0.29	1.00	1.00
P 0.7	0.00	0.00	0.40	0.80	1.00
P 1.0	0.00	0.00	0.40	1.00	1.00
P	0.11	0.15	0.54	0.98	1.00
Total	0.10	0.14	0.54	0.99	1.00

Table 53. Uncensored Vendor B Raw Breakdown Data.

	Field										
	8	9	10	11	12	13	14	15	16	17	18
0.1	4	2	0	0	2	25	4	0	0	1	1
0.5	0	0	2	0	3	62	1	0	0	0	1
1	0	0	1	0	7	91	0	0	0	0	0
N1 0.1	2	0	0	0	0	8	2	0	0	1	1
N1 0.5	0	0	0	0	0	9	0	0	0	0	1
N1 1.0	0	0	0	0	0	24	0	0	0	0	0
N1	2	0	0	0	0	41	2	0	0	1	2
N2 0.1	0	0	0	0	0	4	0	0	0	0	0
N2 0.5	0	0	1	0	2	19	0	0	0	0	0
N2 1.0	0	0	1	0	5	22	0	0	0	0	0
N2	0	0	2	0	7	45	0	0	0	0	0
N	2	0	2	0	7	86	2	0	0	1	2
P1 0.1	2	2	0	0	1	10	2	0	0	0	0
P1 0.5	0	0	0	0	0	11	1	0	0	0	0
P1 1.0	0	0	0	0	0	22	0	0	0	0	0
P1	2	2	0	0	1	43	3	0	0	0	0
P2 0.1	0	0	0	0	1	3	0	0	0	0	0
P2 0.5	0	0	1	0	1	23	0	0	0	0	0
P2 1.0	0	0	0	0	2	23	0	0	0	0	0
P2	0	0	1	0	4	49	0	0	0	0	0
P	2	2	1	0	5	92	3	0	0	0	0
I 0.1	4	2	0	0	1	18	4	0	0	1	1
I 0.5	0	0	0	0	0	20	1	0	0	0	1
I 1.0	0	0	0	0	0	46	0	0	0	0	0
I	4	2	0	0	1	84	5	0	0	1	2
II 0.1	0	0	0	0	1	7	0	0	0	0	0
II 0.5	0	0	2	0	3	42	0	0	0	0	0
II 1.0	0	0	1	0	7	45	0	0	0	0	0
II	0	0	3	0	11	94	0	0	0	0	0
Total	4	2	3	0	12	178	5	0	0	1	2

Table 54. Uncensored Vendor B Cumulative Breakdown Data.

	Field										
	8	9	10	11	12	13	14	15	16	17	18
0.1	0.10	0.15	0.15	0.15	0.21	0.85	0.95	0.95	0.95	0.97	1.00
0.5	0.00	0.00	0.03	0.03	0.07	0.97	0.99	0.99	0.99	0.99	1.00
1	0.00	0.00	0.01	0.01	0.08	1.00	1.00	1.00	1.00	1.00	1.00
N1 0.1	0.14	0.14	0.14	0.14	0.14	0.71	0.86	0.86	0.86	0.93	1.00
N1 0.5	0.00	0.00	0.00	0.00	0.00	0.90	0.90	0.90	0.90	0.90	1.00
N1 1.0	0.00	0.00	0.00	0.00	0.00	1.00	1.00	1.00	1.00	1.00	1.00
N1	0.04	0.04	0.04	0.04	0.04	0.90	0.94	0.94	0.94	0.96	1.00
N2 0.1	0.00	0.00	0.00	0.00	0.00	1.00	1.00	1.00	1.00	1.00	1.00
N2 0.5	0.00	0.00	0.05	0.05	0.14	1.00	1.00	1.00	1.00	1.00	1.00
N2 1.0	0.00	0.00	0.04	0.04	0.21	1.00	1.00	1.00	1.00	1.00	1.00
N2	0.00	0.00	0.04	0.04	0.17	1.00	1.00	1.00	1.00	1.00	1.00
N	0.02	0.02	0.04	0.04	0.11	0.95	0.97	0.97	0.97	0.98	1.00
P1 0.1	0.12	0.24	0.24	0.24	0.29	0.88	1.00	1.00	1.00	1.00	1.00
P1 0.5	0.00	0.00	0.00	0.00	0.00	0.92	1.00	1.00	1.00	1.00	1.00
P1 1.0	0.00	0.00	0.00	0.00	0.00	1.00	1.00	1.00	1.00	1.00	1.00
P1	0.04	0.08	0.08	0.08	0.10	0.94	1.00	1.00	1.00	1.00	1.00
P2 0.1	0.00	0.00	0.00	0.00	0.25	1.00	1.00	1.00	1.00	1.00	1.00
P2 0.5	0.00	0.00	0.04	0.04	0.08	1.00	1.00	1.00	1.00	1.00	1.00
P2 1.0	0.00	0.00	0.00	0.00	0.08	1.00	1.00	1.00	1.00	1.00	1.00
P2	0.00	0.00	0.02	0.02	0.09	1.00	1.00	1.00	1.00	1.00	1.00
P	0.02	0.04	0.05	0.05	0.10	0.97	1.00	1.00	1.00	1.00	1.00
I 0.1	0.13	0.19	0.19	0.19	0.23	0.81	0.94	0.94	0.94	0.97	1.00
I 0.5	0.00	0.00	0.00	0.00	0.00	0.91	0.95	0.95	0.95	0.95	1.00
I 1.0	0.00	0.00	0.00	0.00	0.00	1.00	1.00	1.00	1.00	1.00	1.00
I	0.04	0.06	0.06	0.06	0.07	0.92	0.97	0.97	0.97	0.98	1.00
II 0.1	0.00	0.00	0.00	0.00	0.13	1.00	1.00	1.00	1.00	1.00	1.00
II 0.5	0.00	0.00	0.04	0.04	0.11	1.00	1.00	1.00	1.00	1.00	1.00
II 1.0	0.00	0.00	0.02	0.02	0.15	1.00	1.00	1.00	1.00	1.00	1.00
II	0.00	0.00	0.03	0.03	0.13	1.00	1.00	1.00	1.00	1.00	1.00
Total	0.02	0.03	0.04	0.04	0.10	0.96	0.99	0.99	0.99	0.99	1.00

Table 55. Censored Vendor B Raw Breakdown Data.

	Field						
	8	9	10	11	12	13	14
0.1	4	2	0	0	2	25	4
0.5	0	0	2	0	3	62	1
1	0	0	1	0	7	91	0
N1 0.1	2	0	0	0	0	8	2
N1 0.5	0	0	0	0	0	9	0
N1 1.0	0	0	0	0	0	24	0
N1	2	0	0	0	0	41	2
N2 0.1	0	0	0	0	0	4	0
N2 0.5	0	0	1	0	2	19	0
N2 1.0	0	0	1	0	5	22	0
N2	0	0	2	0	7	45	0
N	2	0	2	0	7	86	2
P1 0.1	2	2	0	0	1	10	2
P1 0.5	0	0	0	0	0	11	1
P1 1.0	0	0	0	0	0	22	0
P1	2	2	0	0	1	43	3
P2 0.1	0	0	0	0	1	3	0
P2 0.5	0	0	1	0	1	23	0
P2 1.0	0	0	0	0	2	23	0
P2	0	0	1	0	4	49	0
P	2	2	1	0	5	92	3
I 0.1	4	2	0	0	1	18	4
I 0.5	0	0	0	0	0	20	1
I 1.0	0	0	0	0	0	46	0
I	4	2	0	0	1	84	5
II 0.1	0	0	0	0	1	7	0
II 0.5	0	0	2	0	3	42	0
II 1.0	0	0	1	0	7	45	0
II	0	0	3	0	11	94	0
Total	4	2	3	0	12	178	5

Table 56. Censored Vendor B Cumulative Breakdown Data.

	Field						
	8	9	10	11	12	13	14
0.1	0.11	0.16	0.16	0.16	0.22	0.89	1.00
0.5	0.00	0.00	0.03	0.03	0.07	0.99	1.00
1	0.00	0.00	0.01	0.01	0.08	1.00	1.00
N1 0.1	0.17	0.17	0.17	0.17	0.17	0.83	1.00
N1 0.5	0.00	0.00	0.00	0.00	0.00	1.00	1.00
N1 1.0	0.00	0.00	0.00	0.00	0.00	1.00	1.00
N1	0.04	0.04	0.04	0.04	0.04	0.96	1.00
N2 0.1	0.00	0.00	0.00	0.00	0.00	1.00	1.00
N2 0.5	0.00	0.00	0.05	0.05	0.14	1.00	1.00
N2 1.0	0.00	0.00	0.04	0.04	0.21	1.00	1.00
N2	0.00	0.00	0.04	0.04	0.17	1.00	1.00
N	0.02	0.02	0.04	0.04	0.11	0.98	1.00
P1 0.1	0.12	0.24	0.24	0.24	0.29	0.88	1.00
P1 0.5	0.00	0.00	0.00	0.00	0.00	0.92	1.00
P1 1.0	0.00	0.00	0.00	0.00	0.00	1.00	1.00
P1	0.04	0.08	0.08	0.08	0.10	0.94	1.00
P2 0.1	0.00	0.00	0.00	0.00	0.25	1.00	1.00
P2 0.5	0.00	0.00	0.04	0.04	0.08	1.00	1.00
P2 1.0	0.00	0.00	0.00	0.00	0.08	1.00	1.00
P2	0.00	0.00	0.02	0.02	0.09	1.00	1.00
P	0.02	0.04	0.05	0.05	0.10	0.97	1.00
I 0.1	0.14	0.21	0.21	0.21	0.24	0.86	1.00
I 0.5	0.00	0.00	0.00	0.00	0.00	0.95	1.00
I 1.0	0.00	0.00	0.00	0.00	0.00	1.00	1.00
I	0.04	0.06	0.06	0.06	0.07	0.95	1.00
II 0.1	0.00	0.00	0.00	0.00	0.13	1.00	1.00
II 0.5	0.00	0.00	0.04	0.04	0.11	1.00	1.00
II 1.0	0.00	0.00	0.02	0.02	0.15	1.00	1.00
II	0.00	0.00	0.03	0.03	0.13	1.00	1.00
Total	0.02	0.03	0.04	0.04	0.10	0.98	1.00

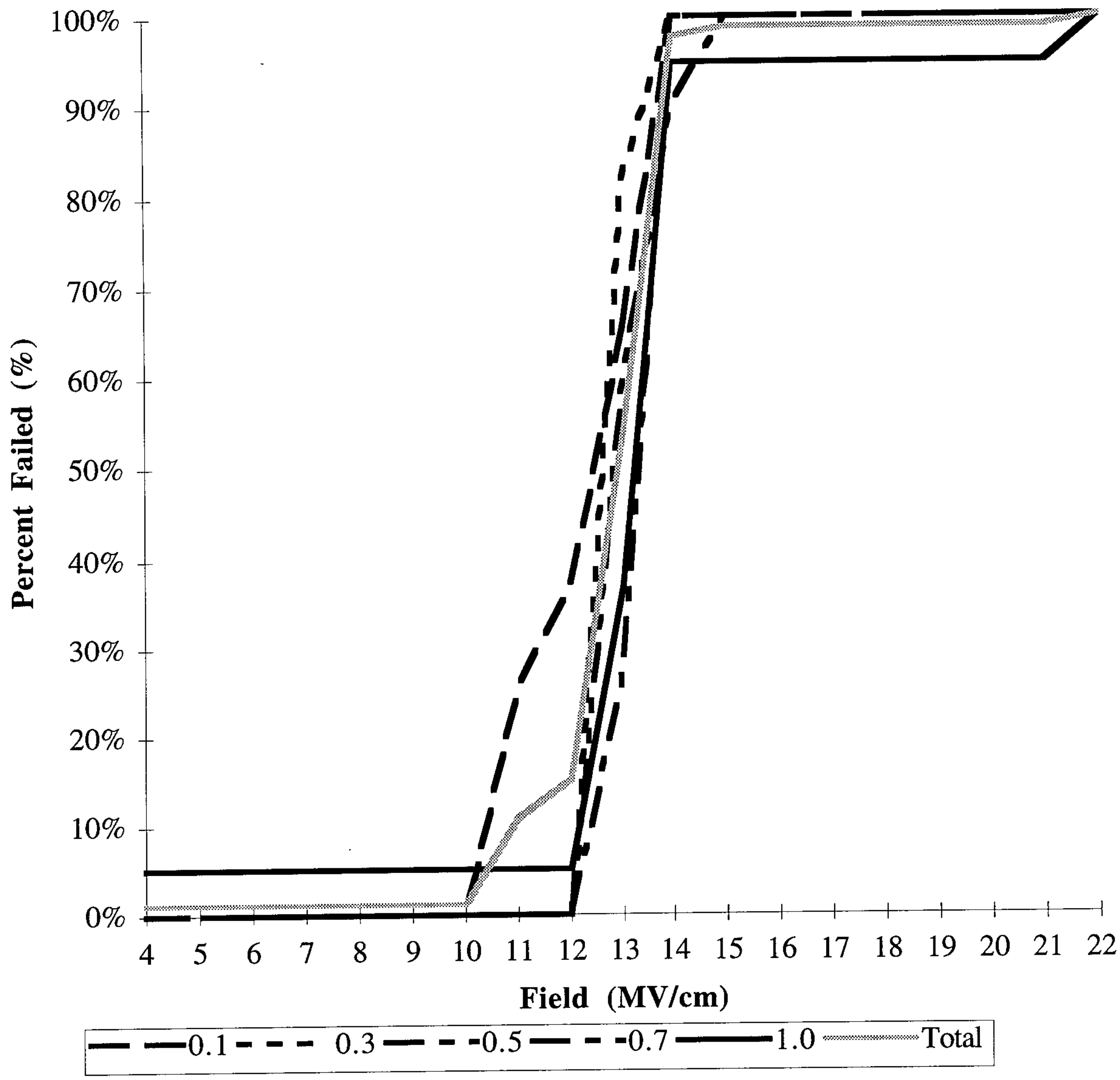

Figure 155. Uncensored Vendor A cumulative breakdown curve by ramp rate.

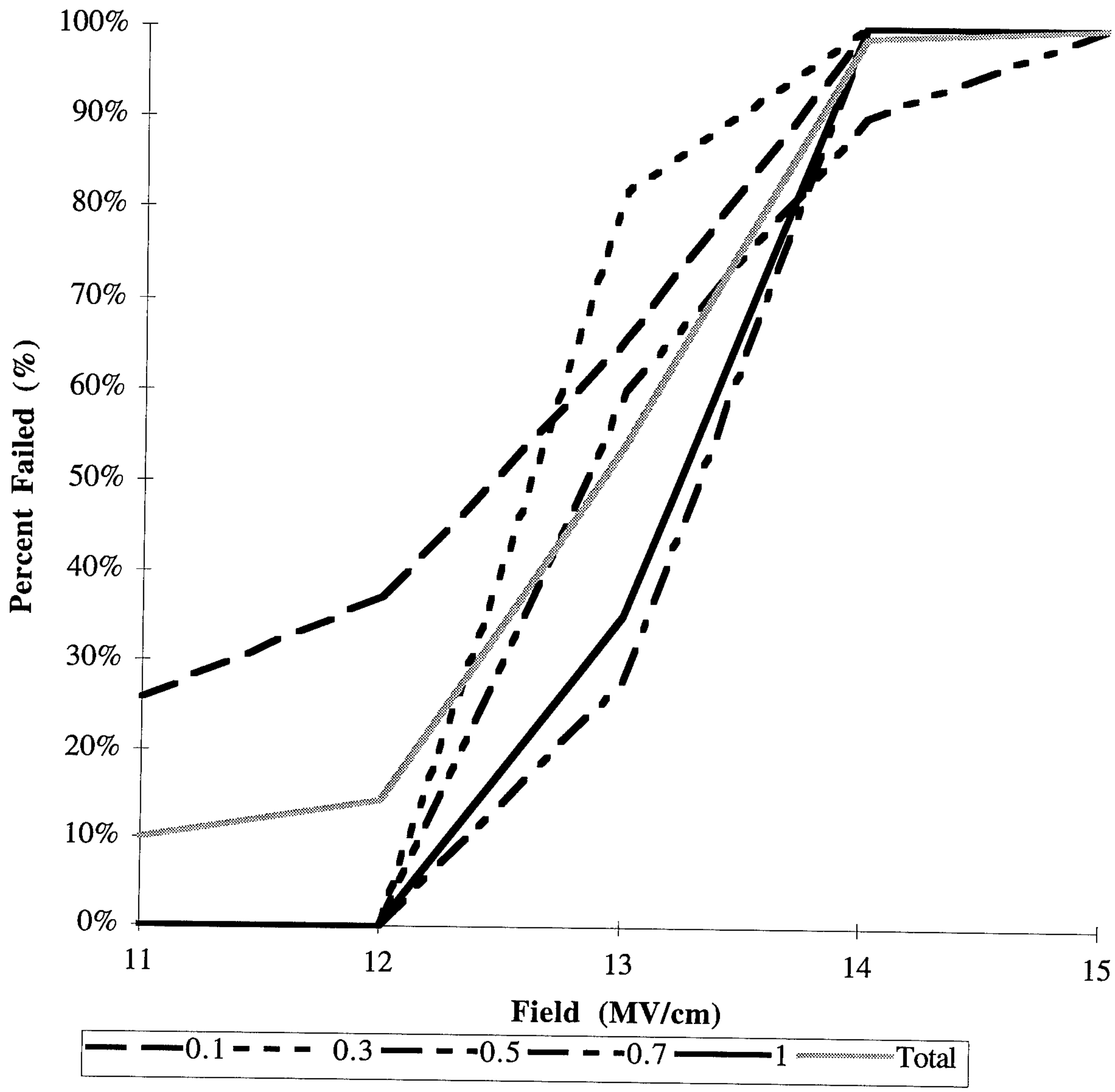

Figure 156. Censored Vendor A cumulative breakdown curve by ramp rate.

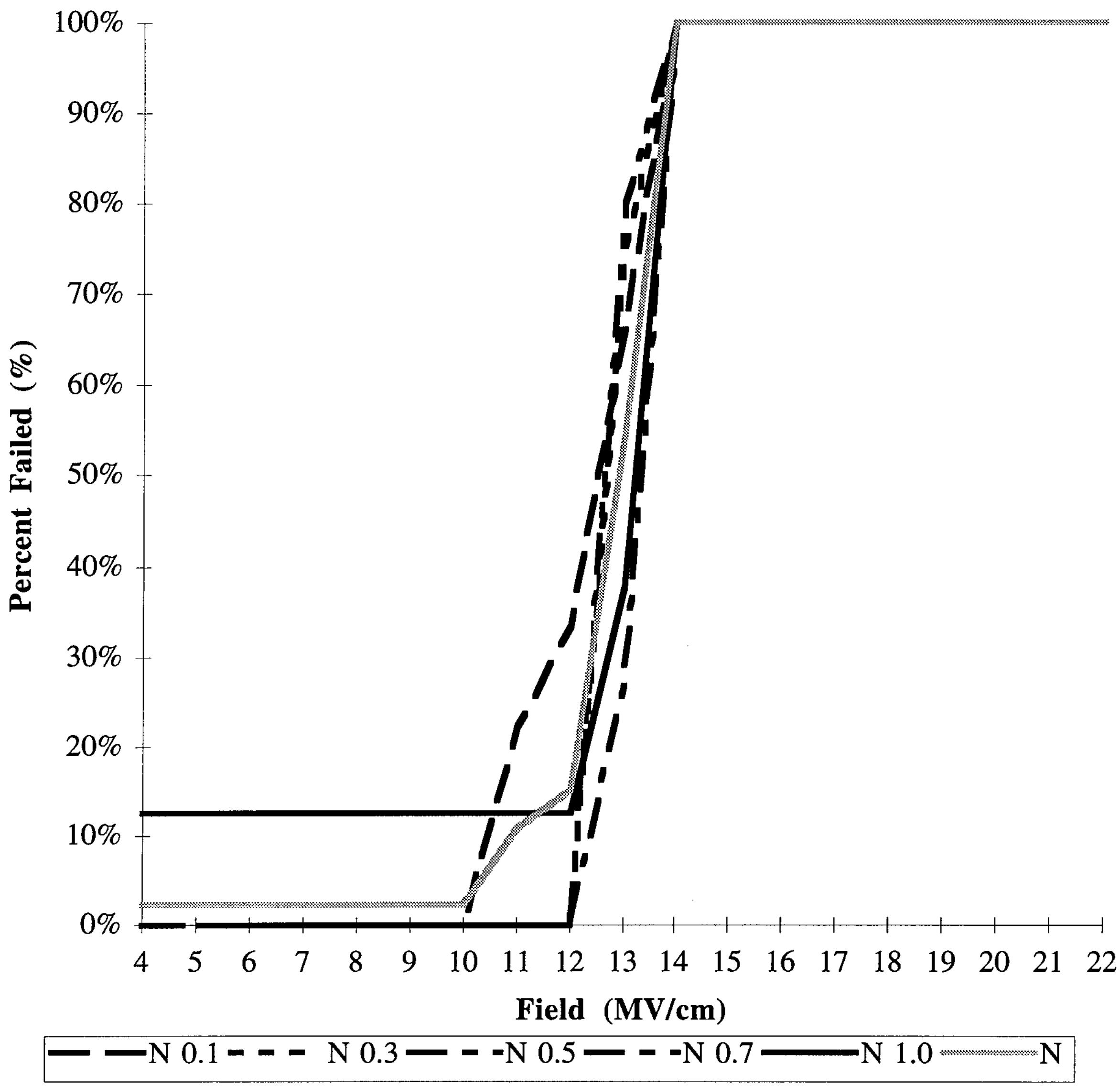

Figure 157. Uncensored Vendor A cumulative breakdown curve for the n capacitors the by ramp rate.

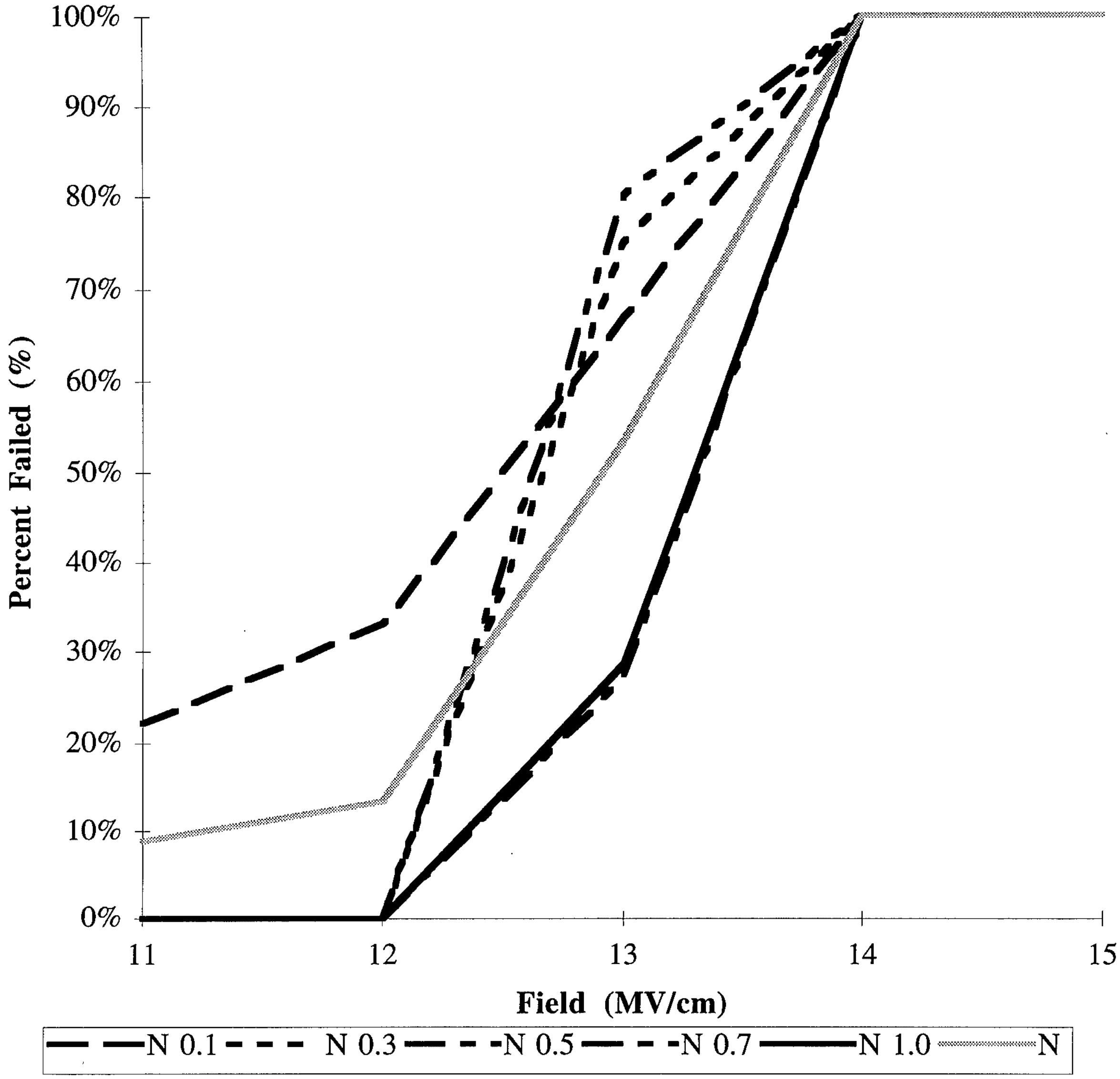

Figure 158. Censored Vendor A cumulative breakdown curve for the n capacitors by the ramp rate.

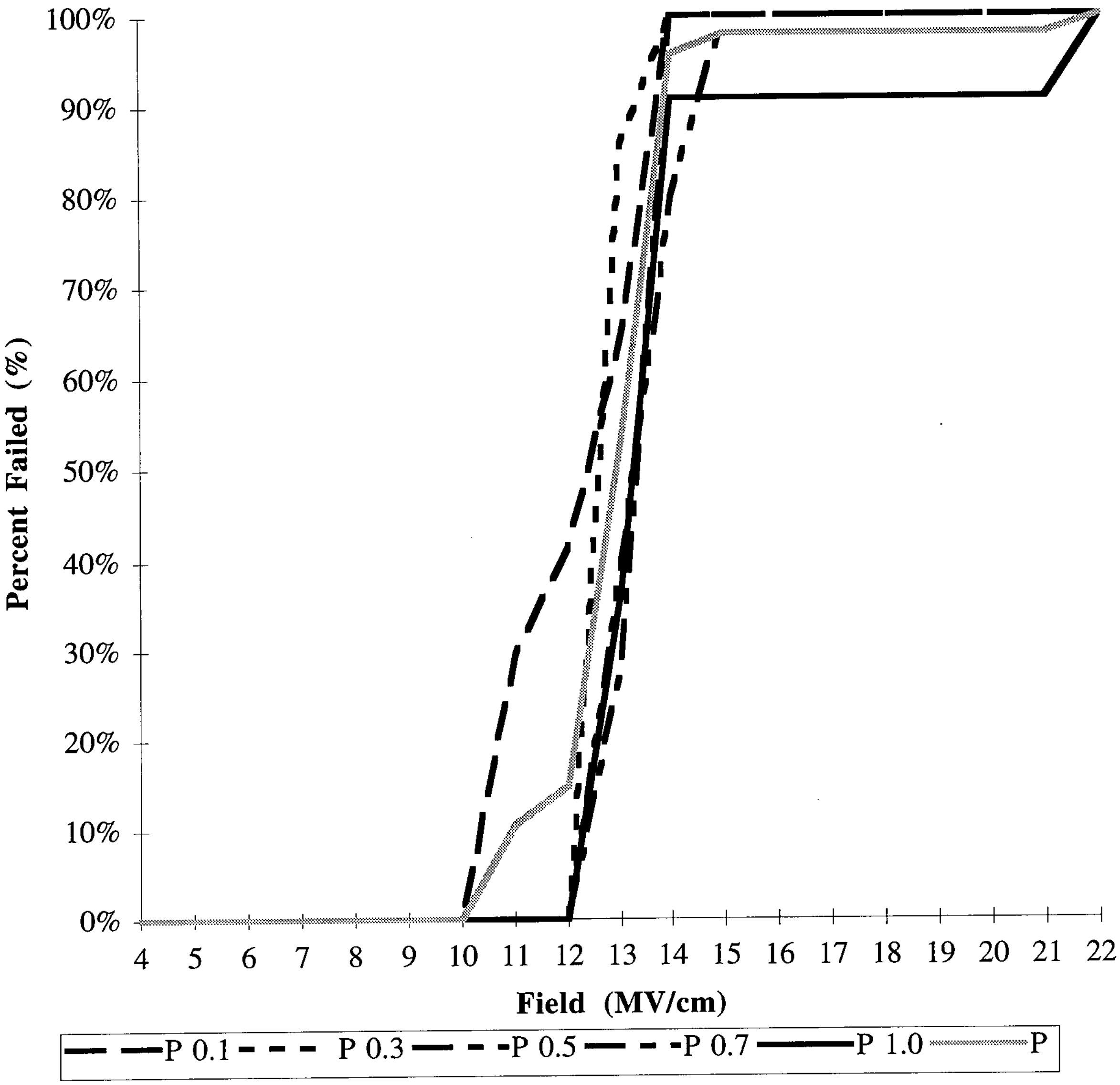

Figure 159. Uncensored Vendor A cumulative breakdown curve for the p capacitors by the ramp rate.

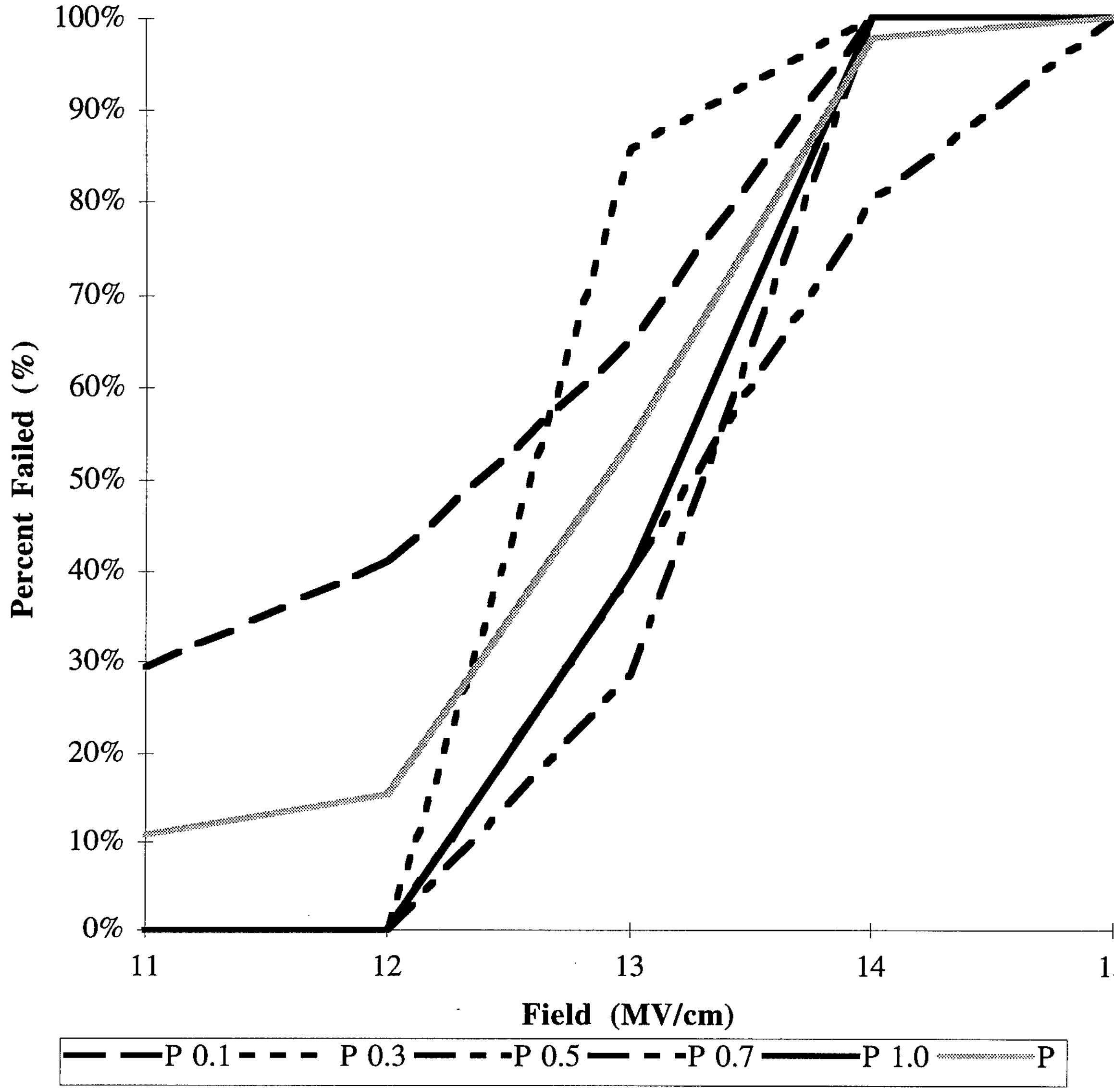

Figure 160. Censored Vendor A cumulative breakdown curve for the p capacitors by the ramp rate.

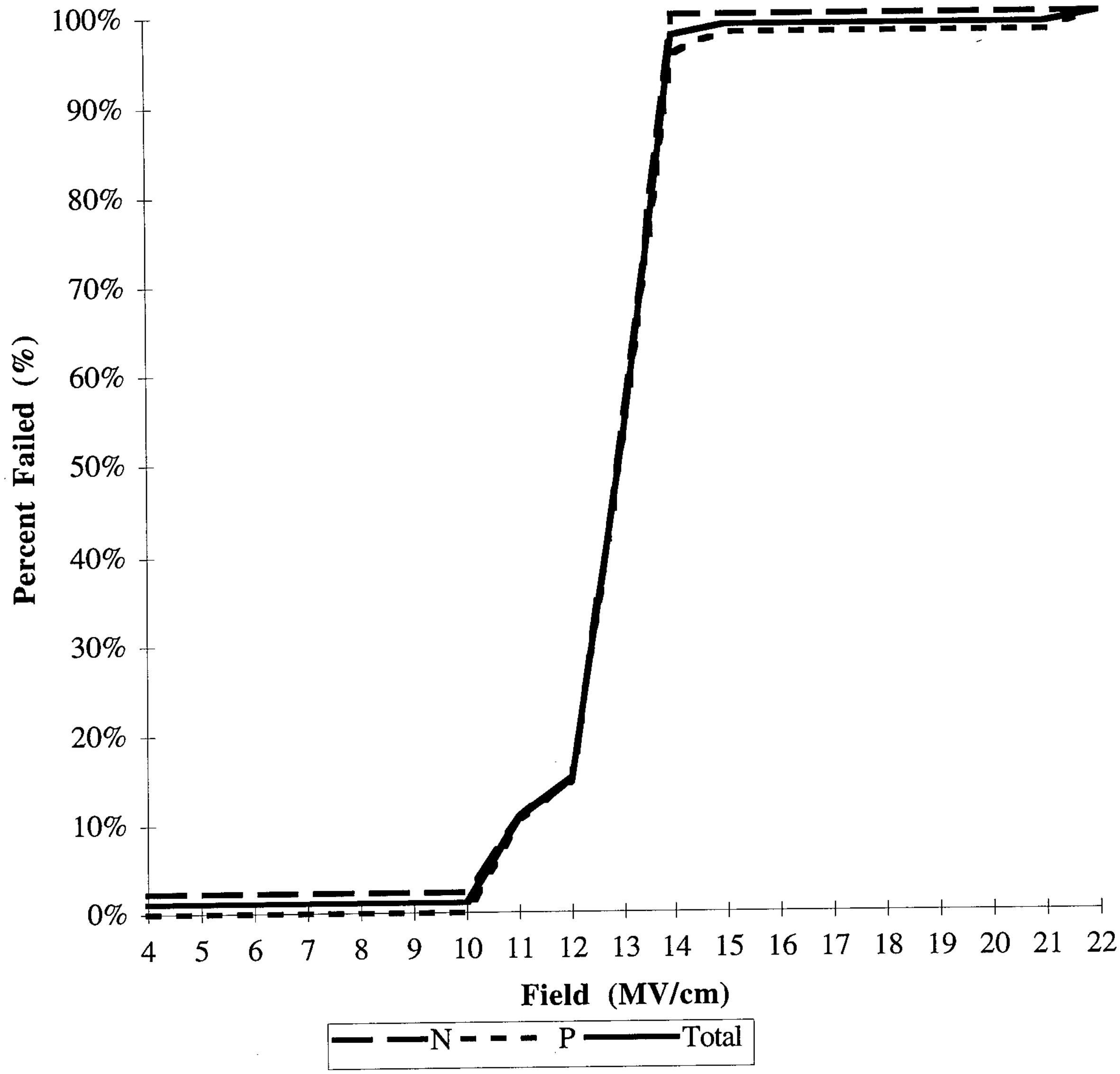

Figure 161. Uncensored Vendor A cumulative breakdown curve by capacitor type.

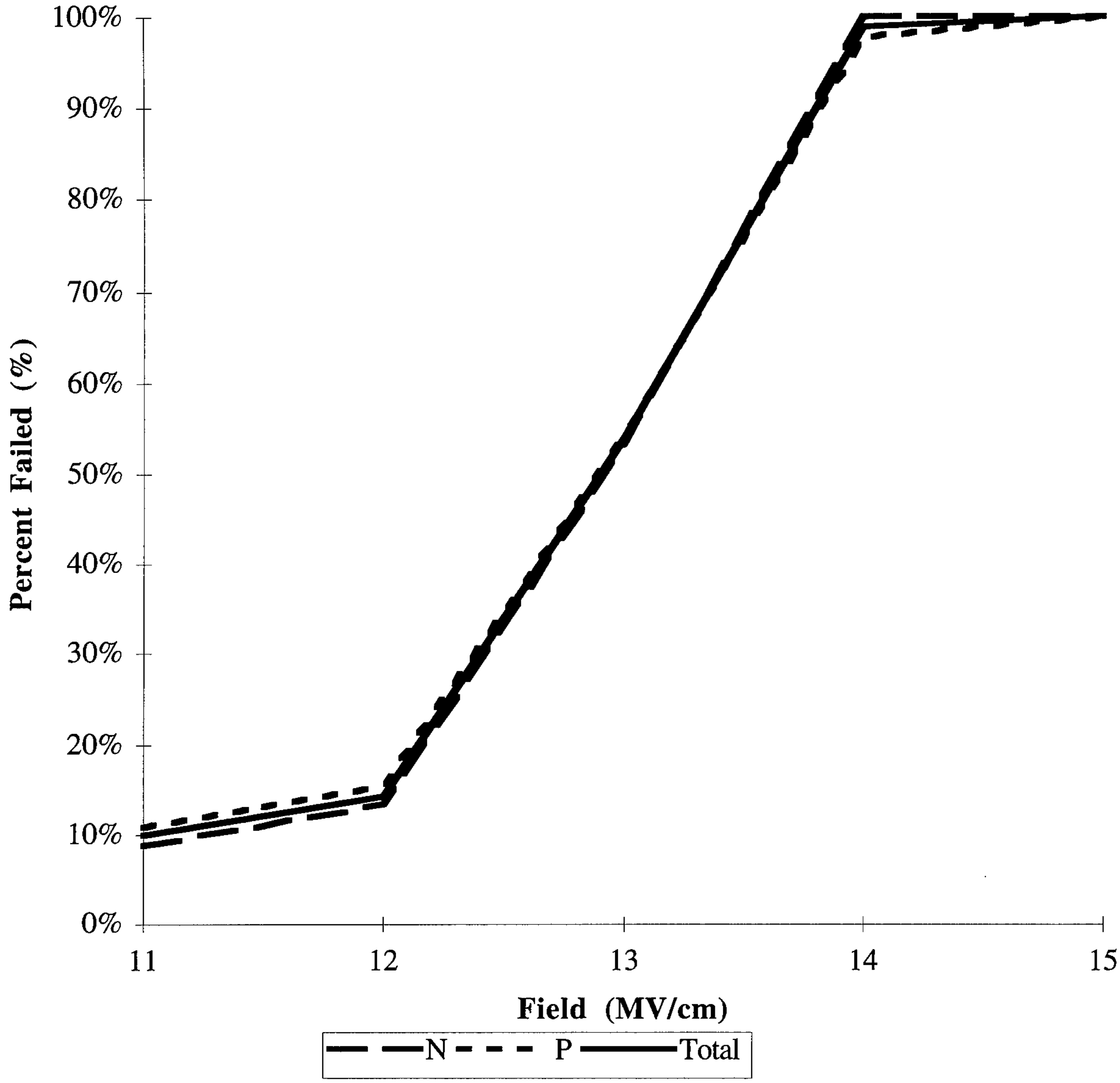

Figure 162. Censored Vendor A cumulative breakdown curve by capacitor type.

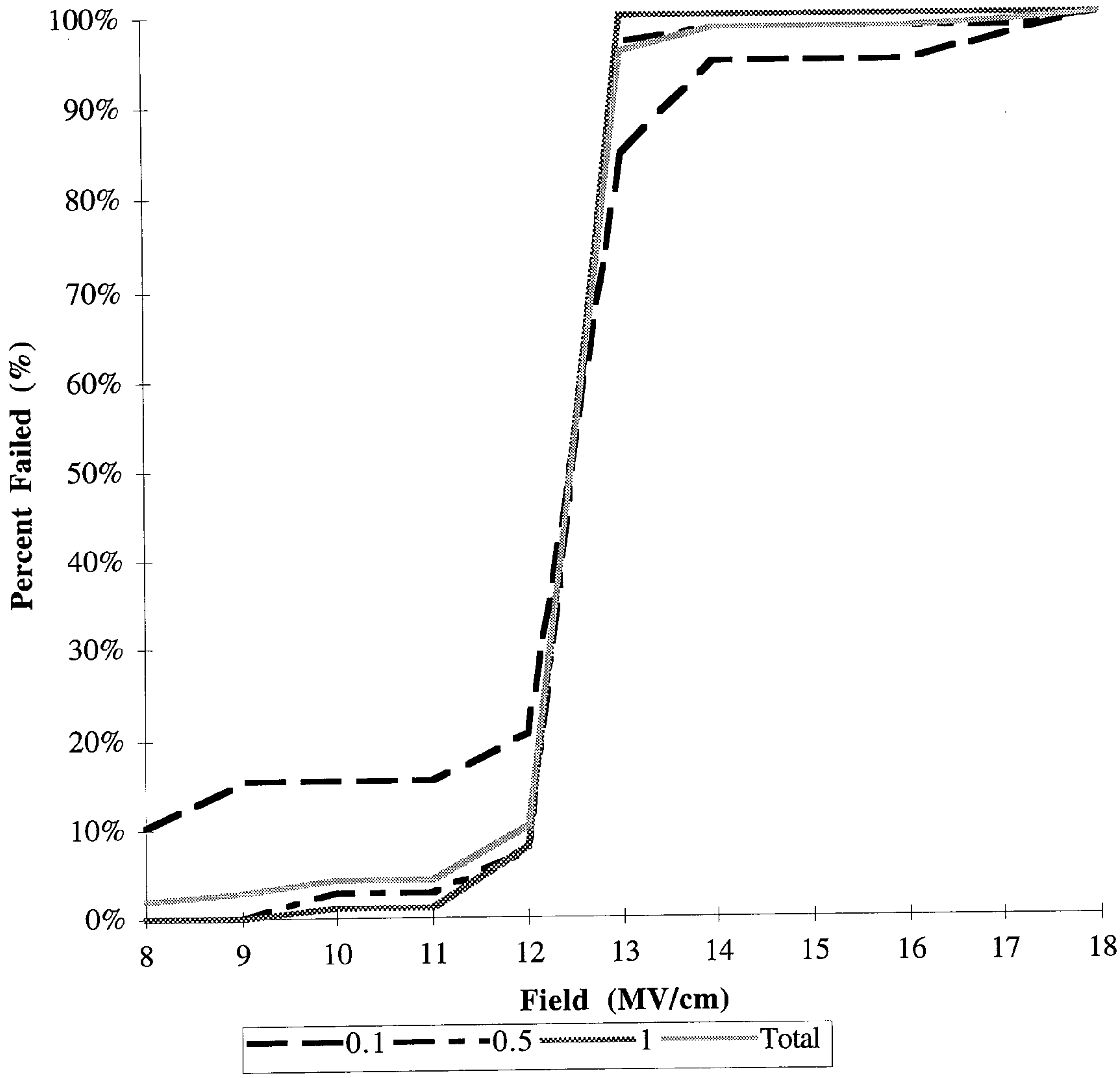

Figure 163. Uncensored Vendor B cumulative breakdown curve by ramp rate.

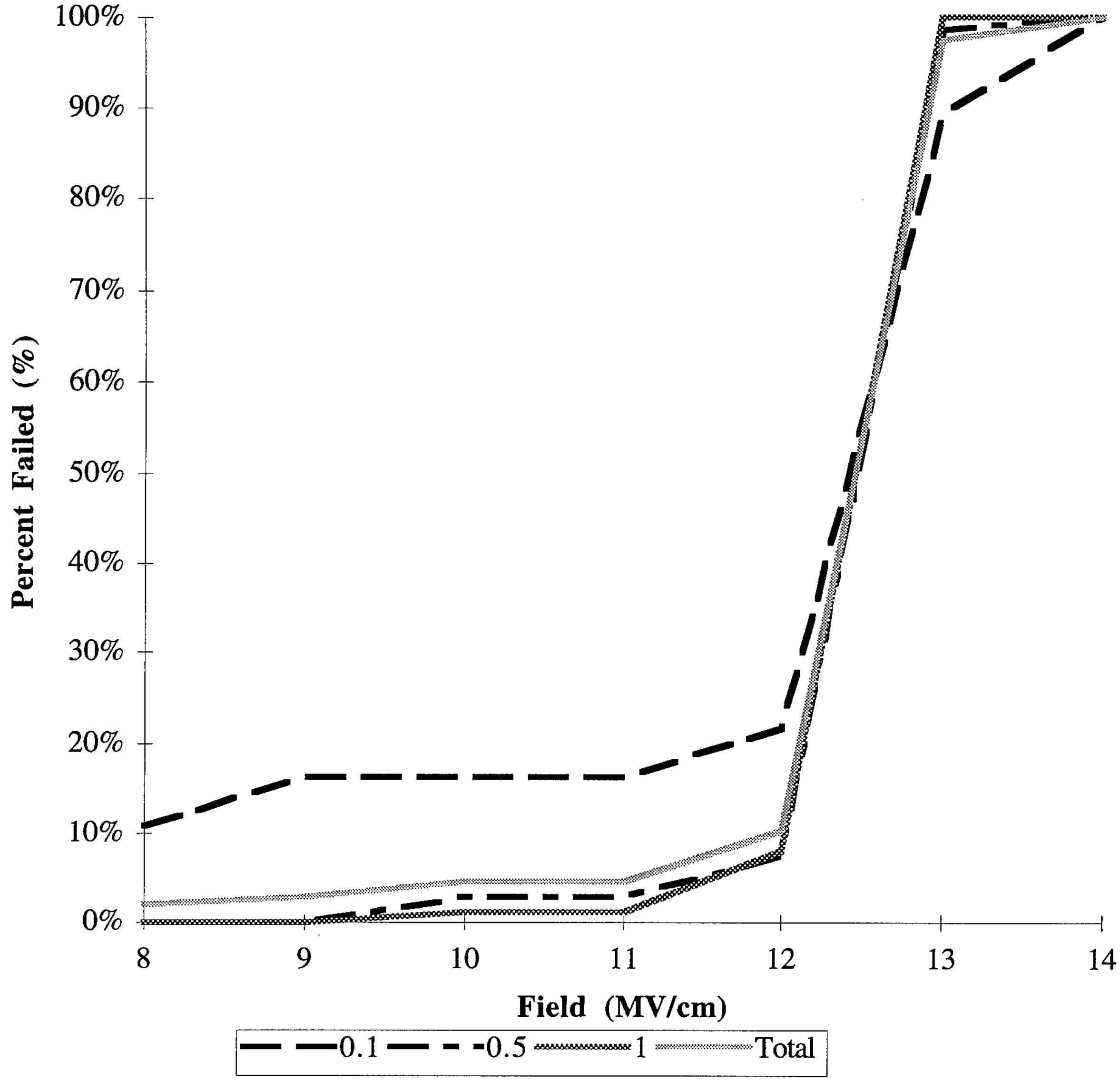

Figure 164. Censored Vendor B cumulative breakdown curve by ramp rate.

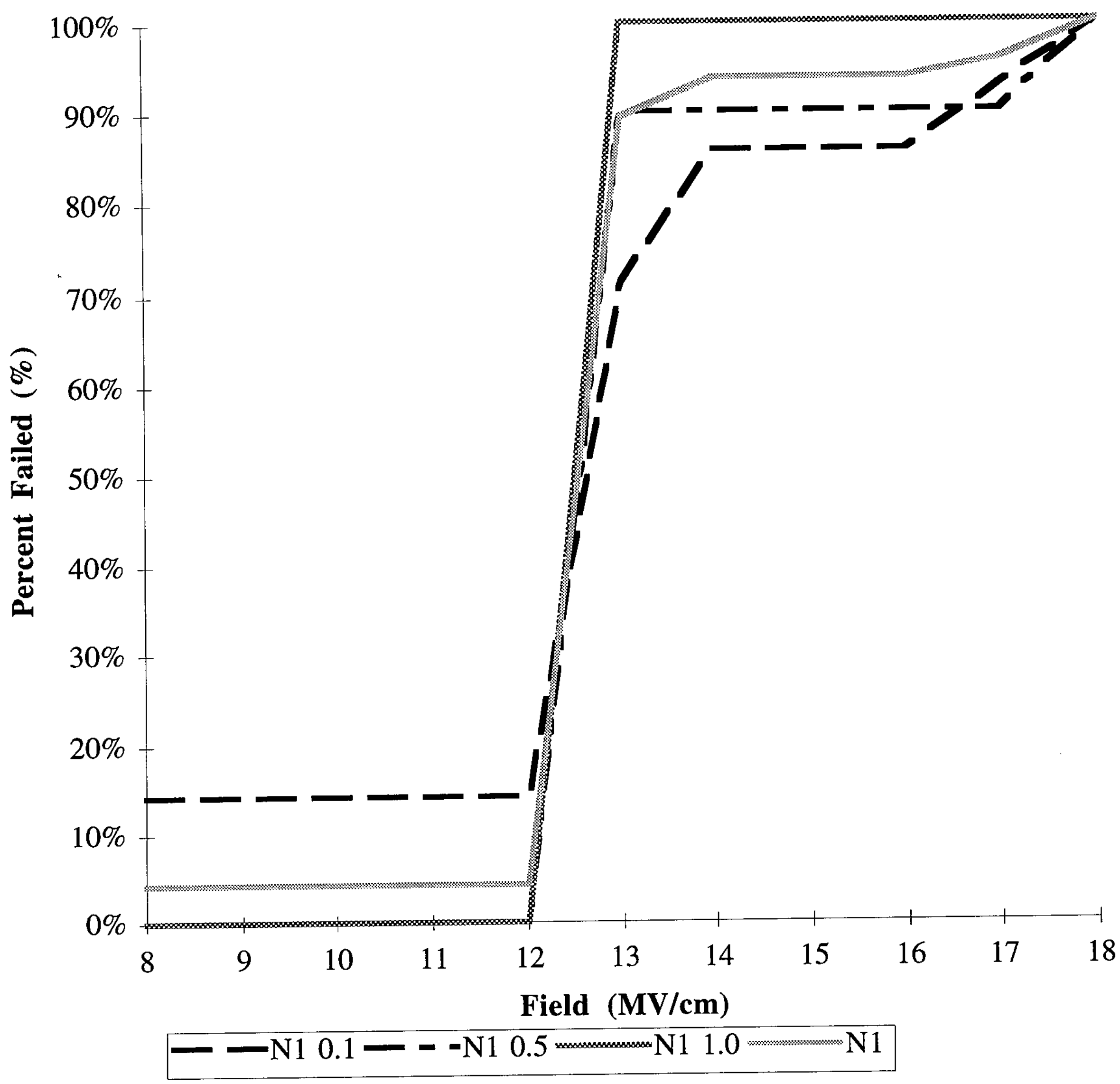

Figure 165. Uncensored Vendor B cumulative breakdown curve for the wafer 1 n capacitors by ramp rate.

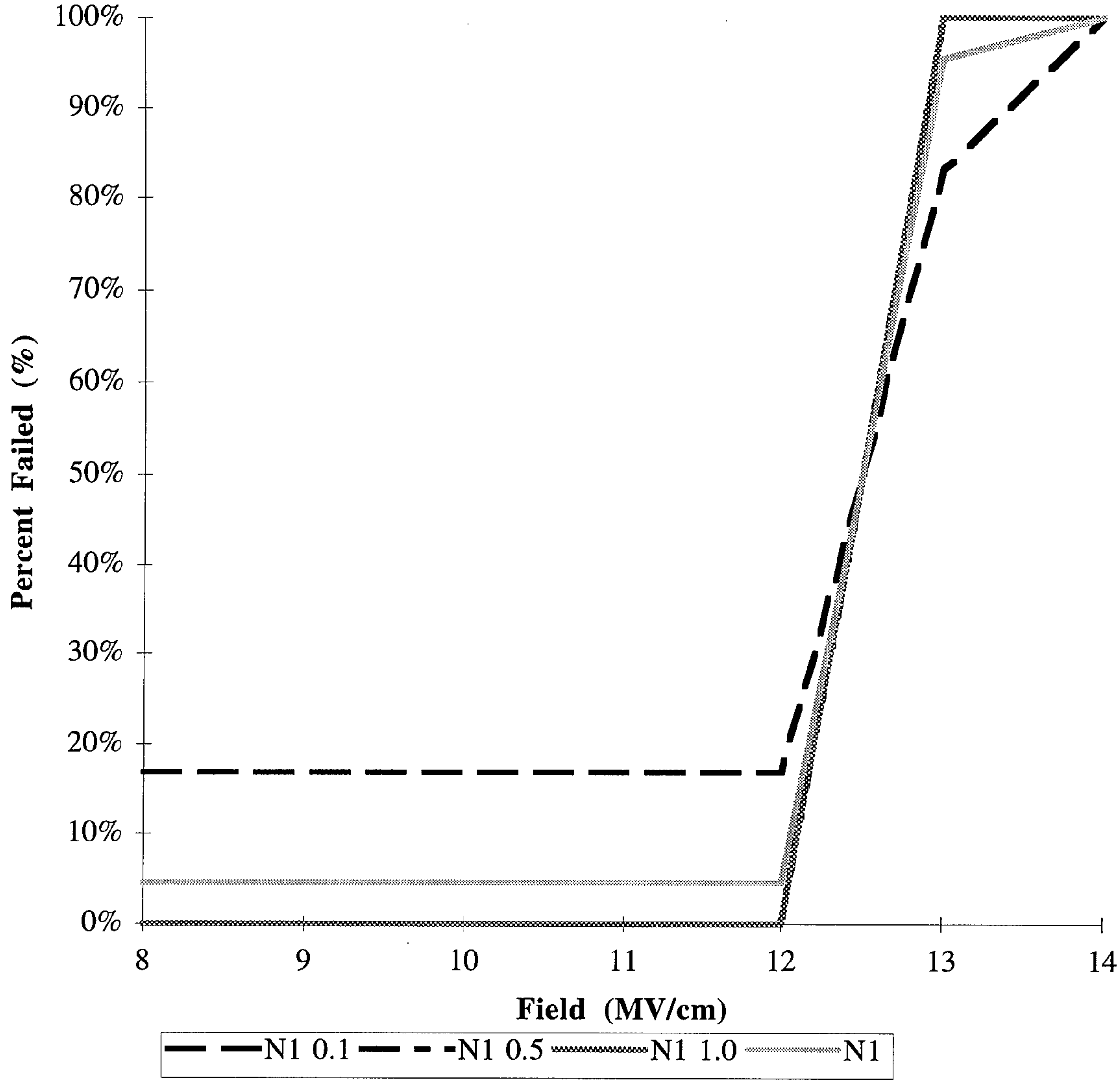

Figure 166. Censored Vendor B cumulative breakdown curve for the wafer 1 n capacitors by ramp rate.

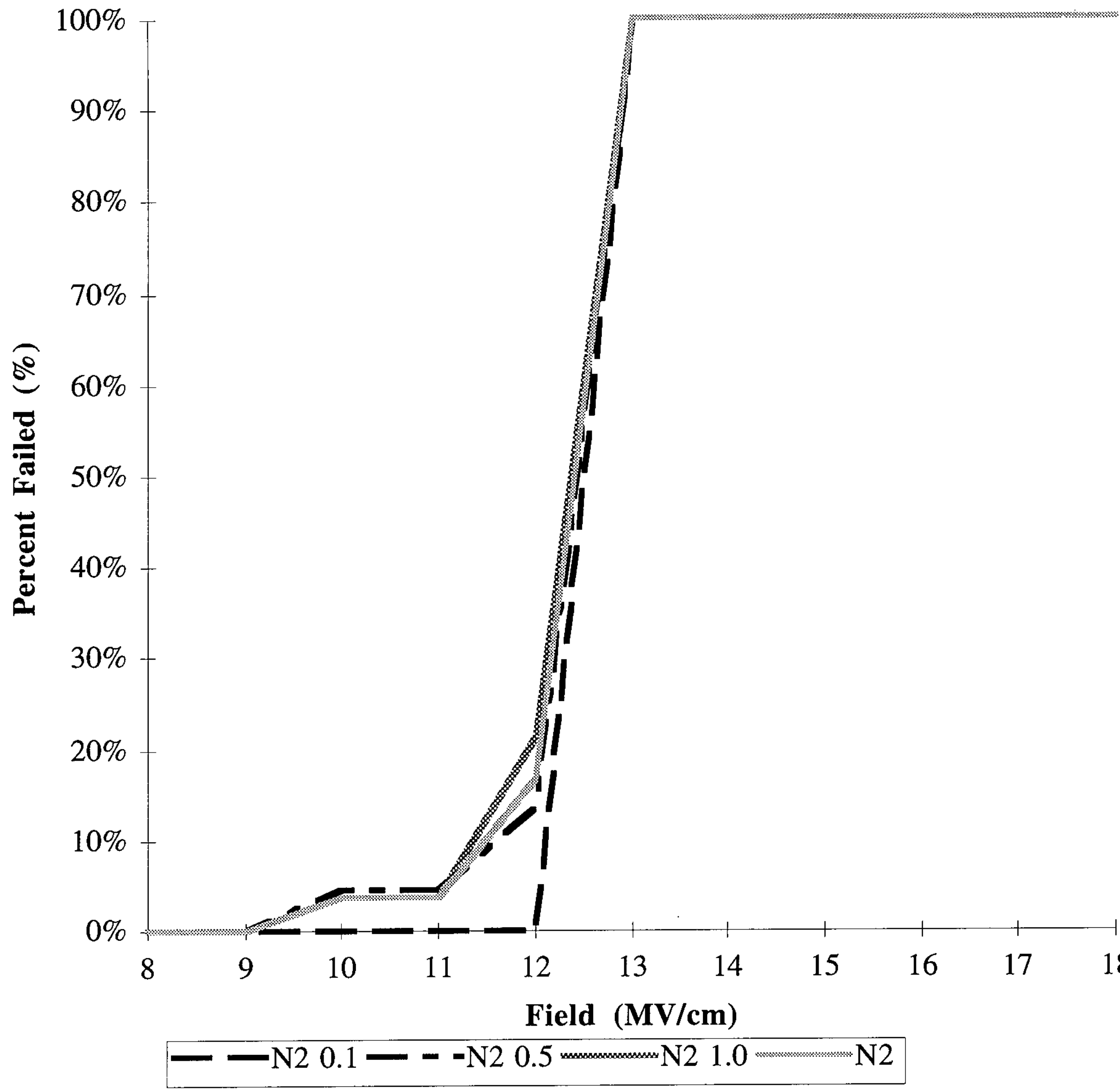

Figure 167. Uncensored Vendor B cumulative breakdown curve for the wafer 2 n capacitors by ramp rate.

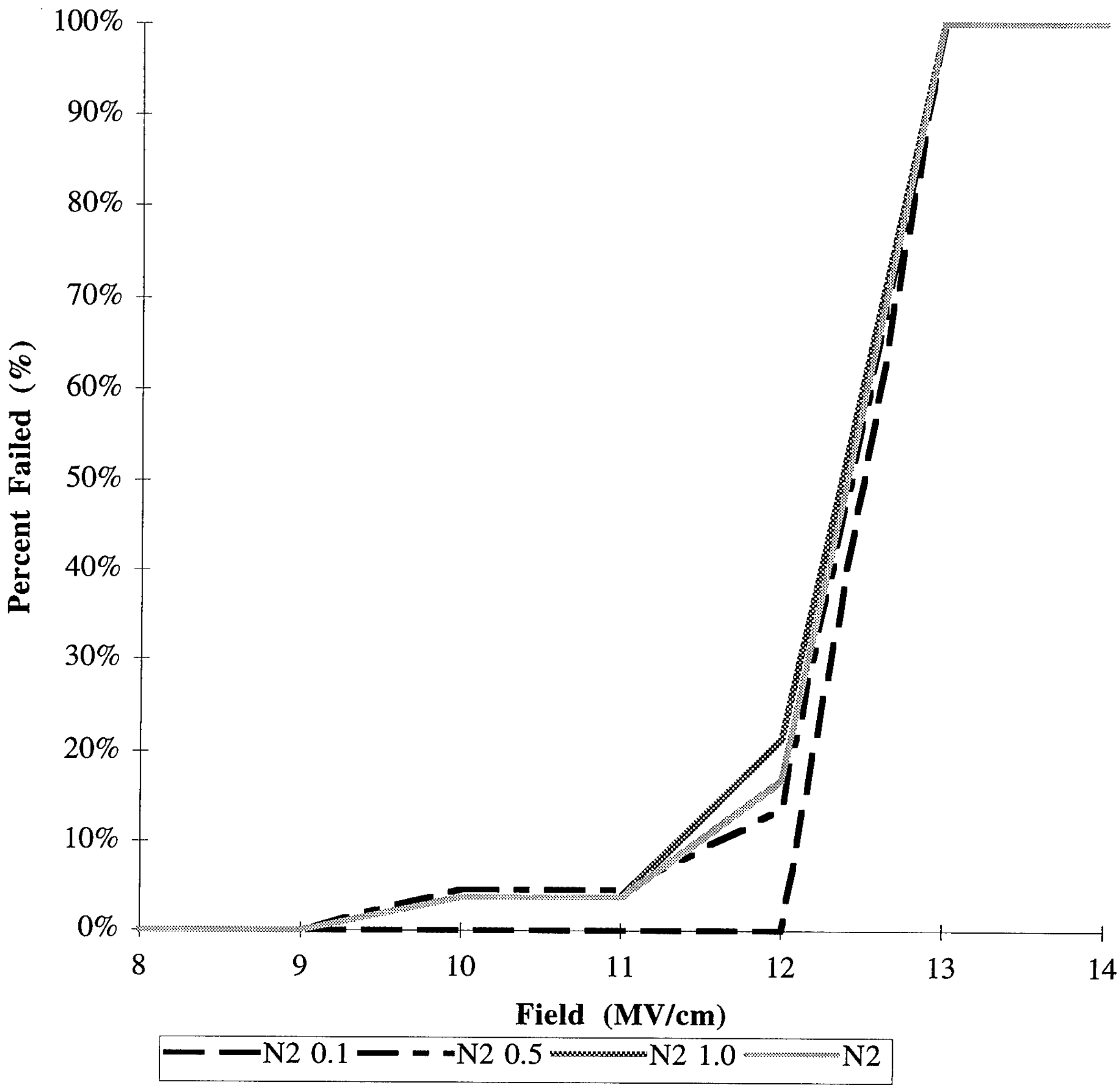

Figure 168. Censored Vendor B cumulative breakdown curve for the wafer 2 n capacitors by ramp rate.

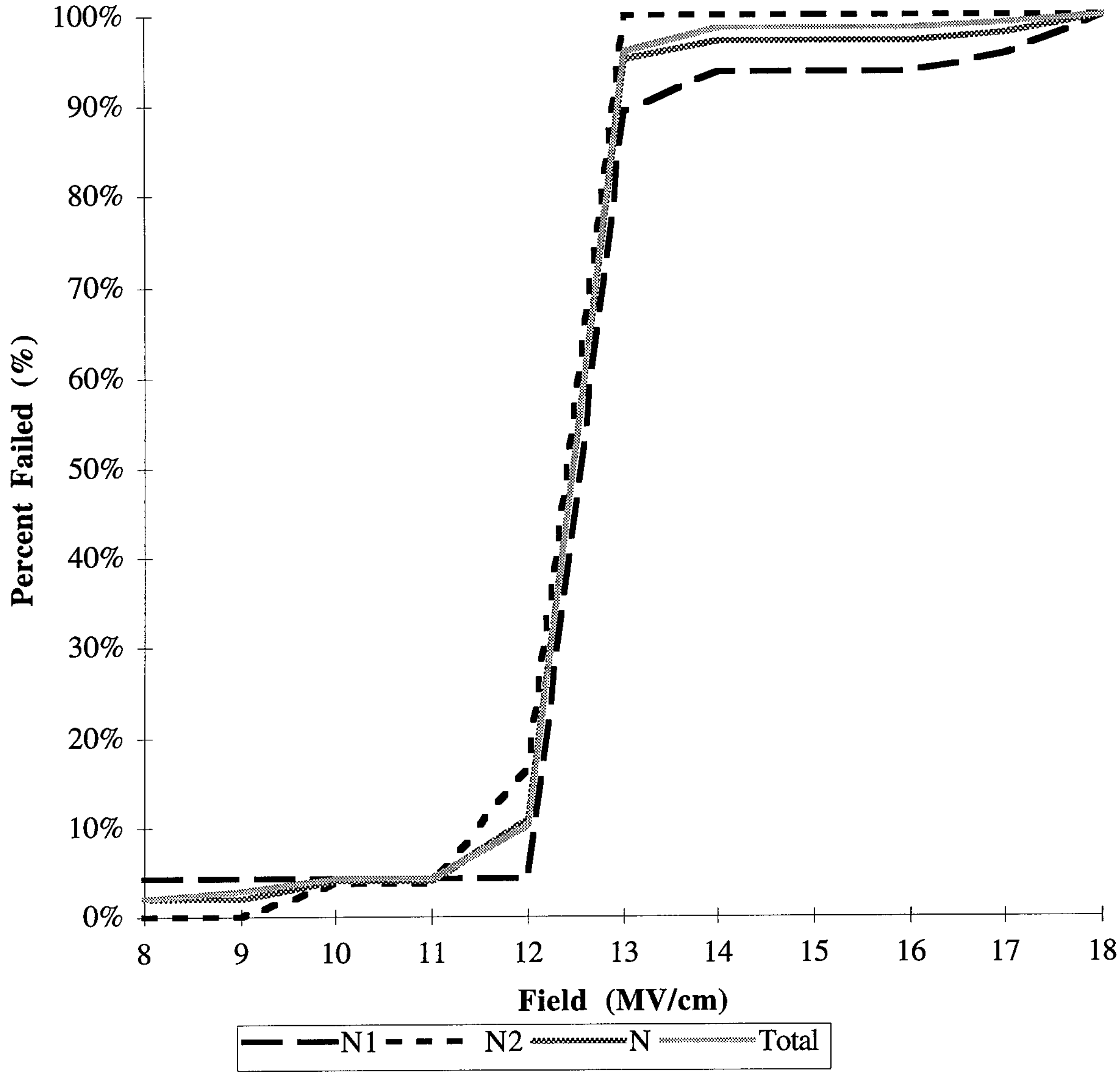

Figure 169. Uncensored Vendor B cumulative breakdown curve for the n capacitors by sample population.

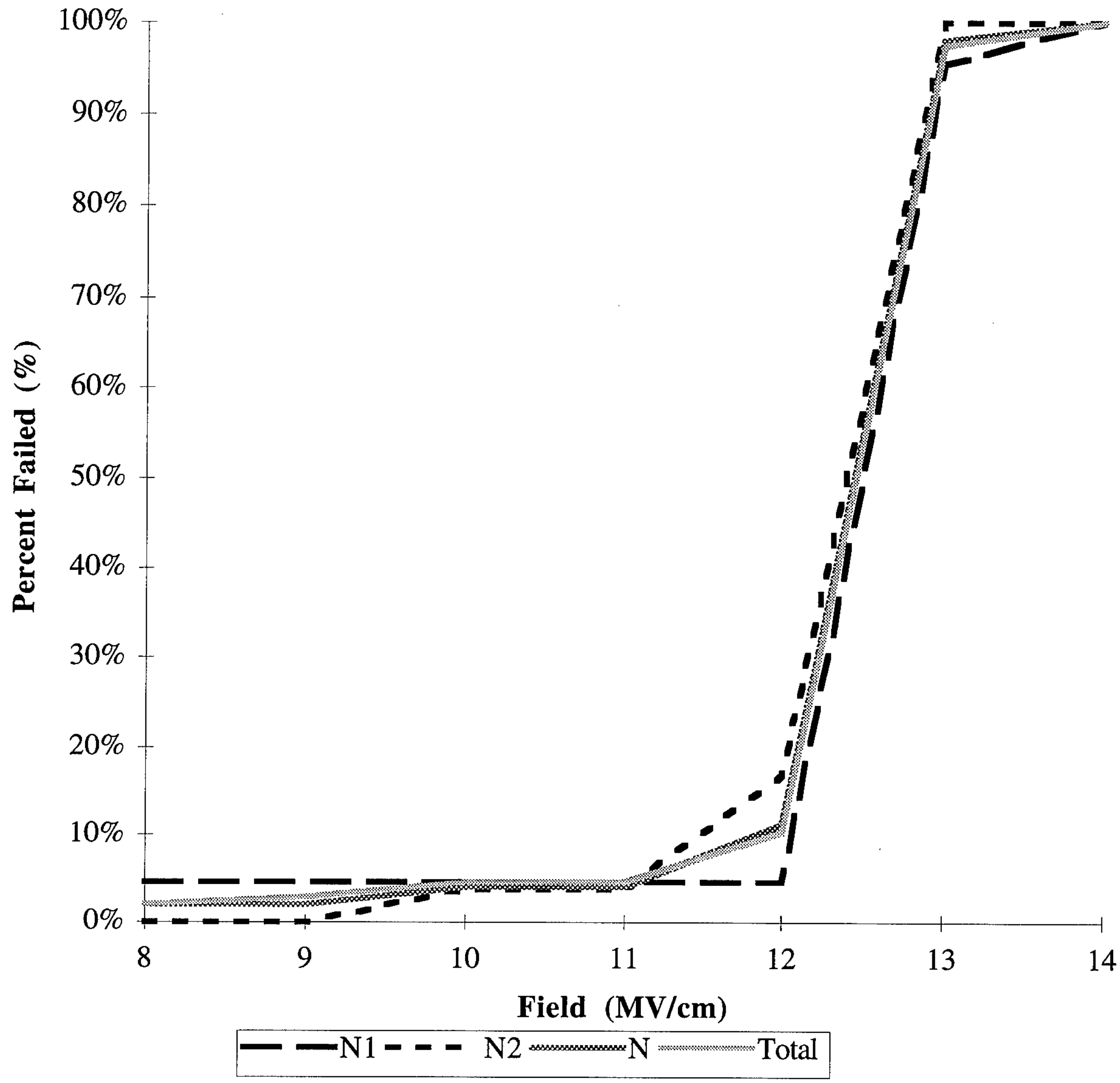

Figure 170. Censored Vendor B cumulative breakdown curve for the n capacitors by sample population.

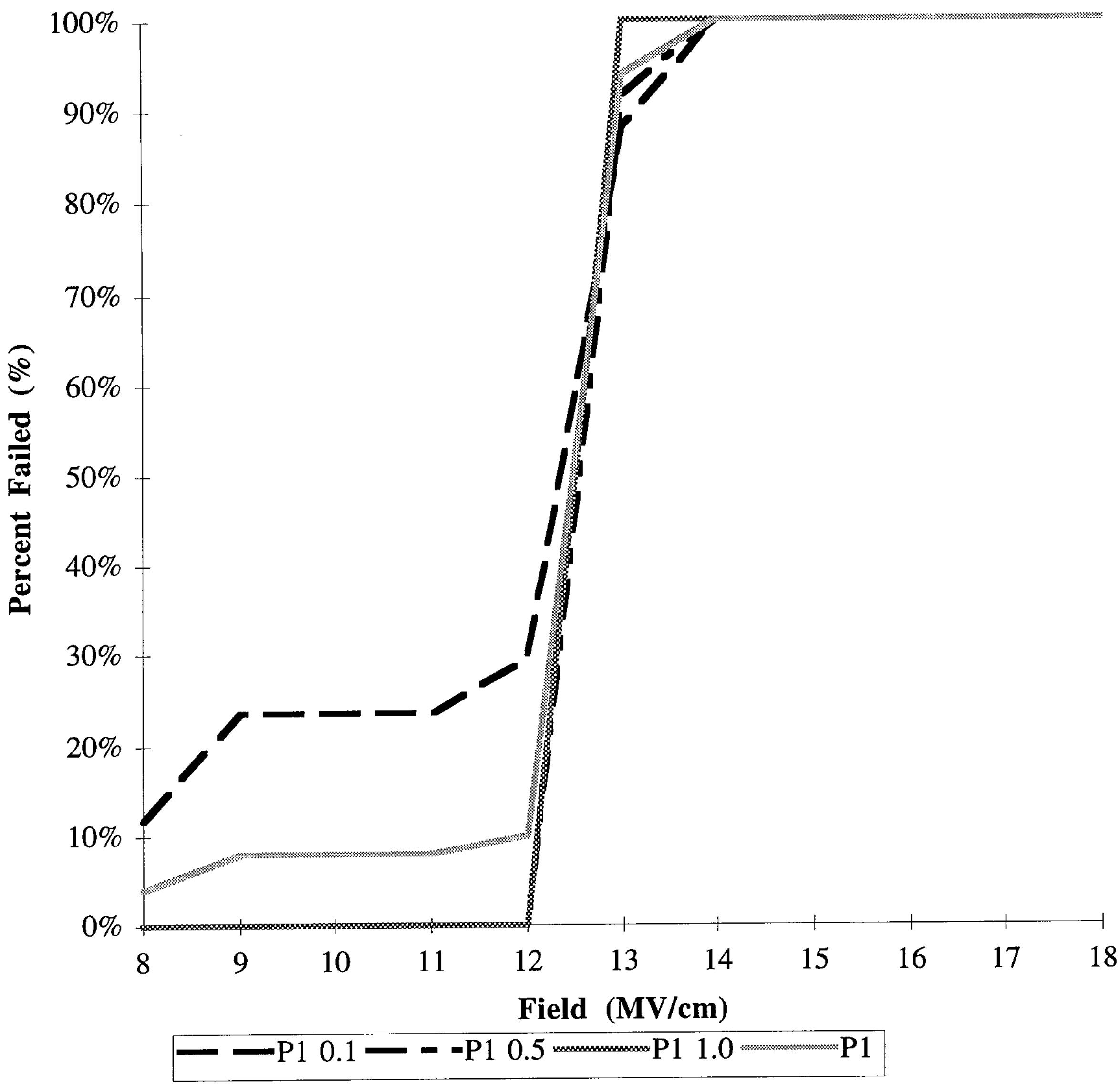

Figure 171. Uncensored Vendor B cumulative breakdown curve for the wafer 1 p capacitors by ramp rate.

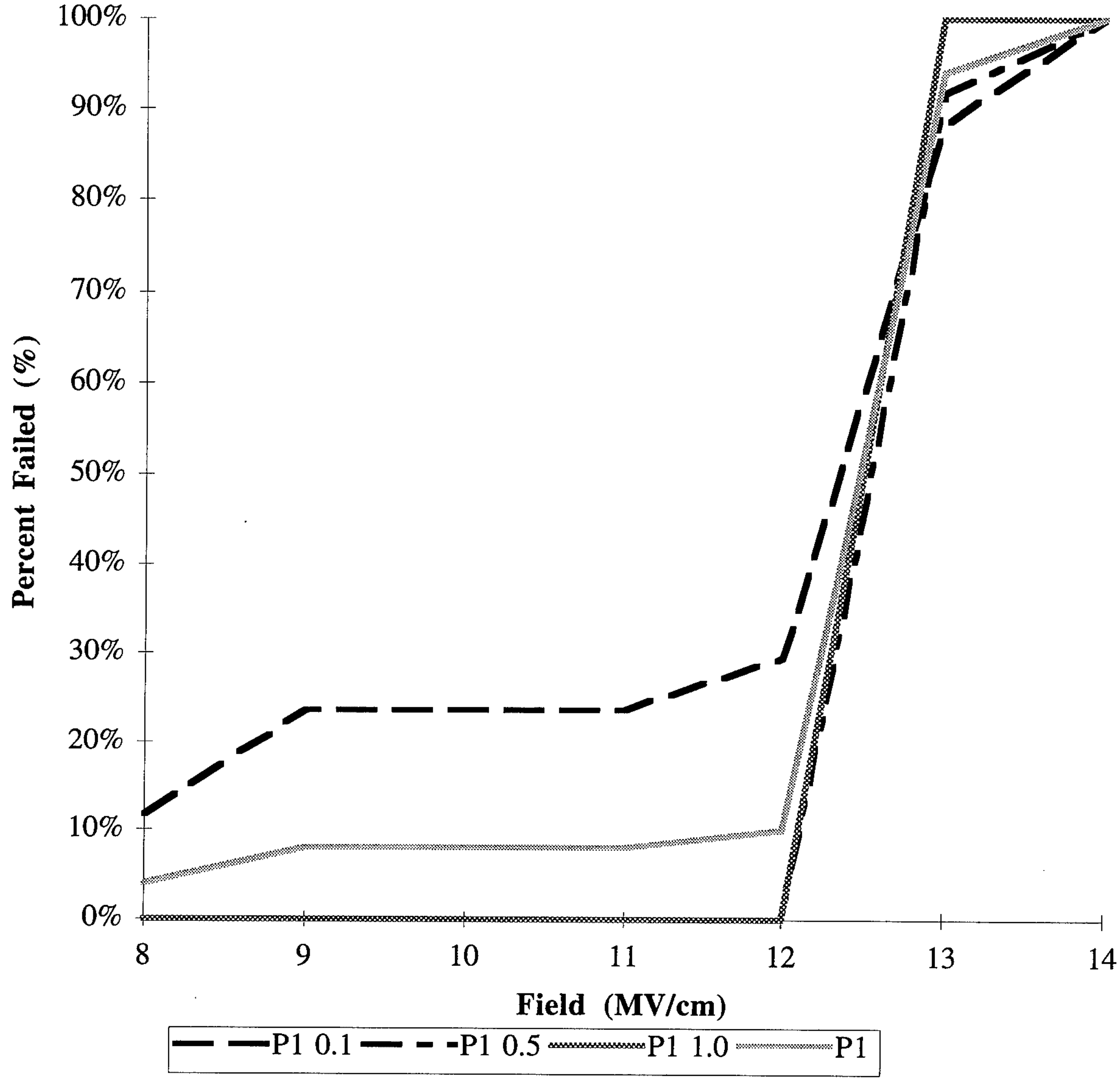

Figure 172. Censored Vendor B cumulative breakdown curve for the wafer 1 p capacitors by ramp rate.

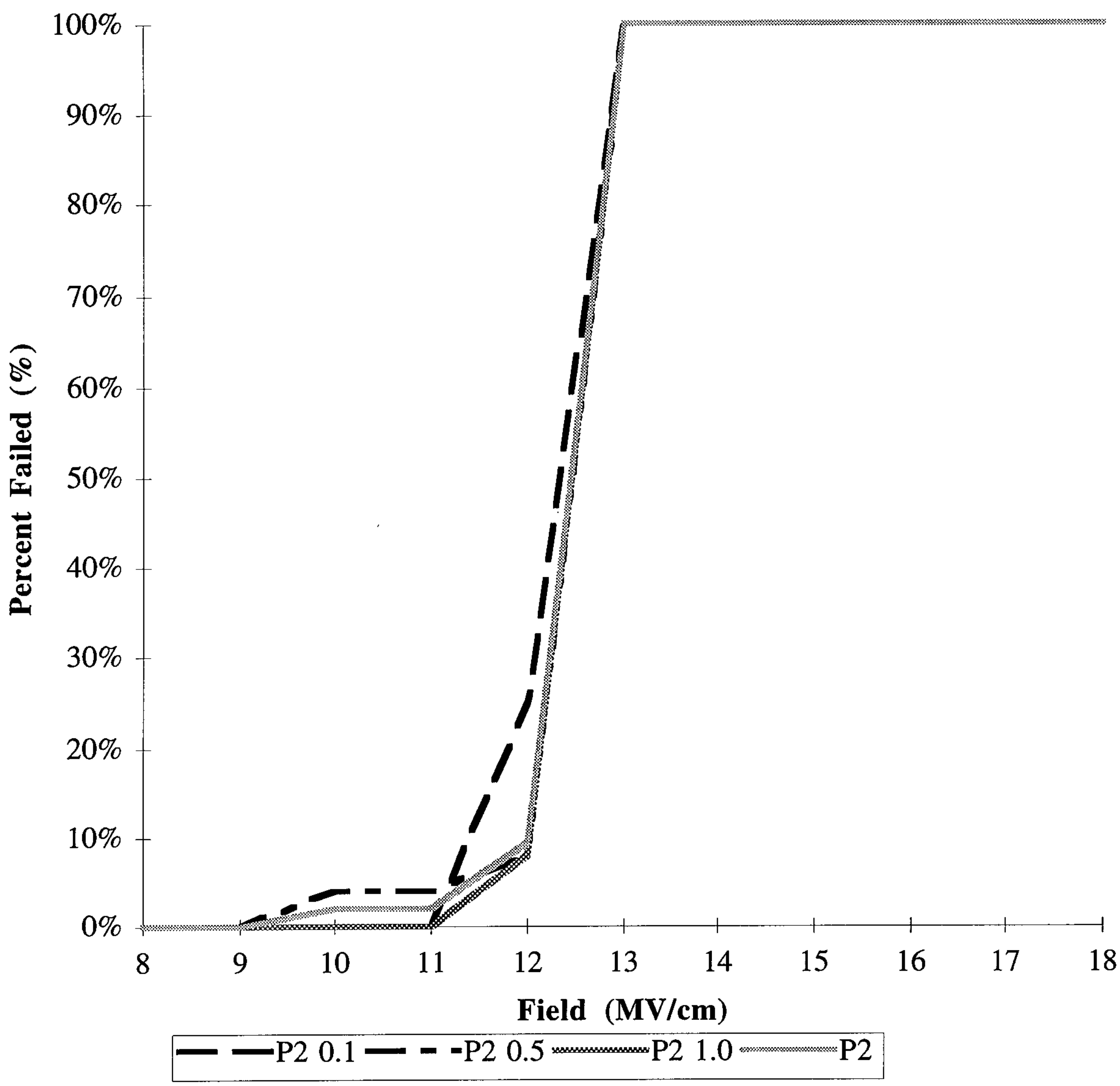

Figure 173. Uncensored Vendor B cumulative breakdown curve for the wafer 2 p capacitors by ramp rate.

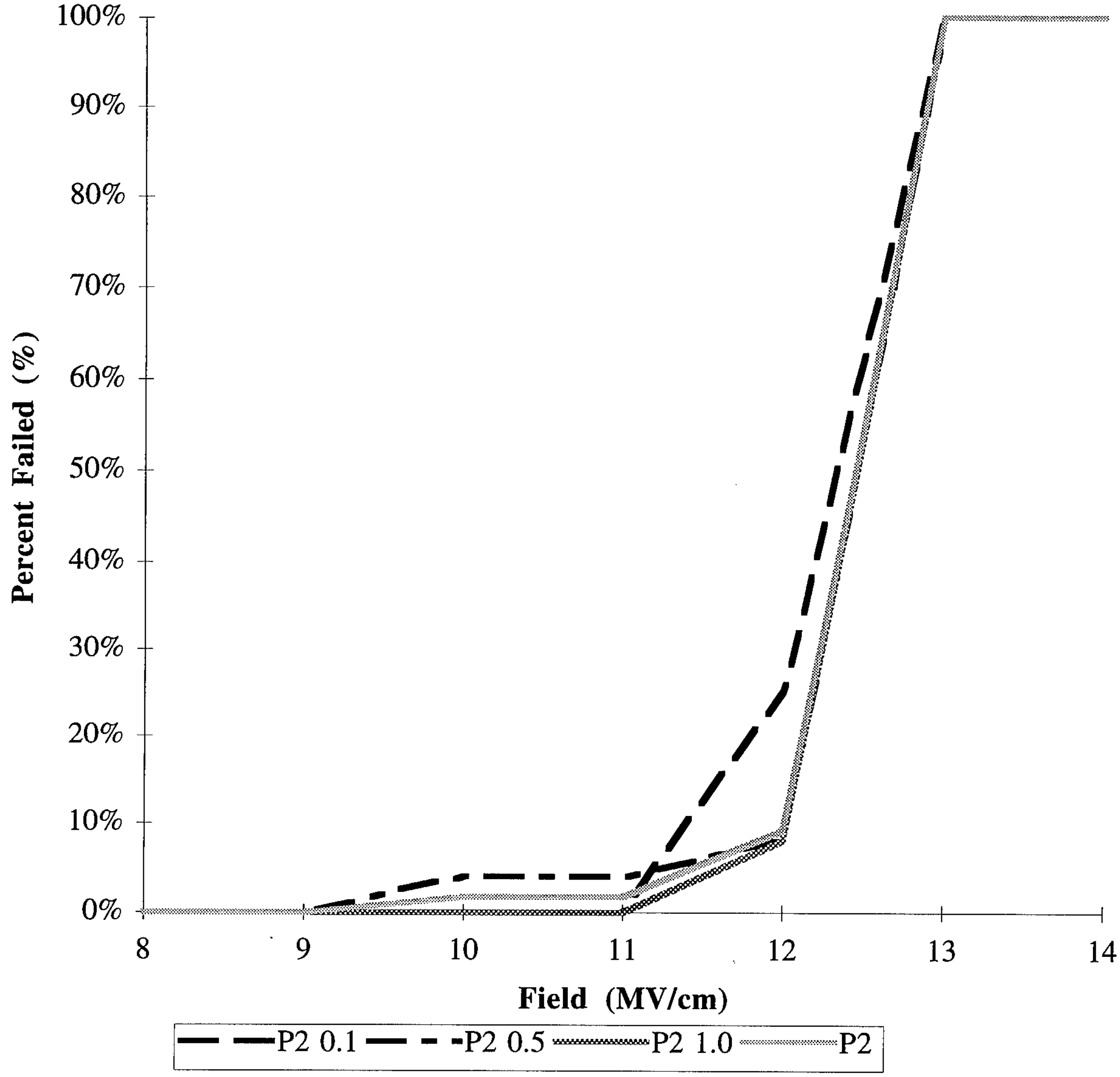

Figure 174. Censored Vendor B cumulative breakdown curve for the wafer 2 p capacitors by ramp rate.

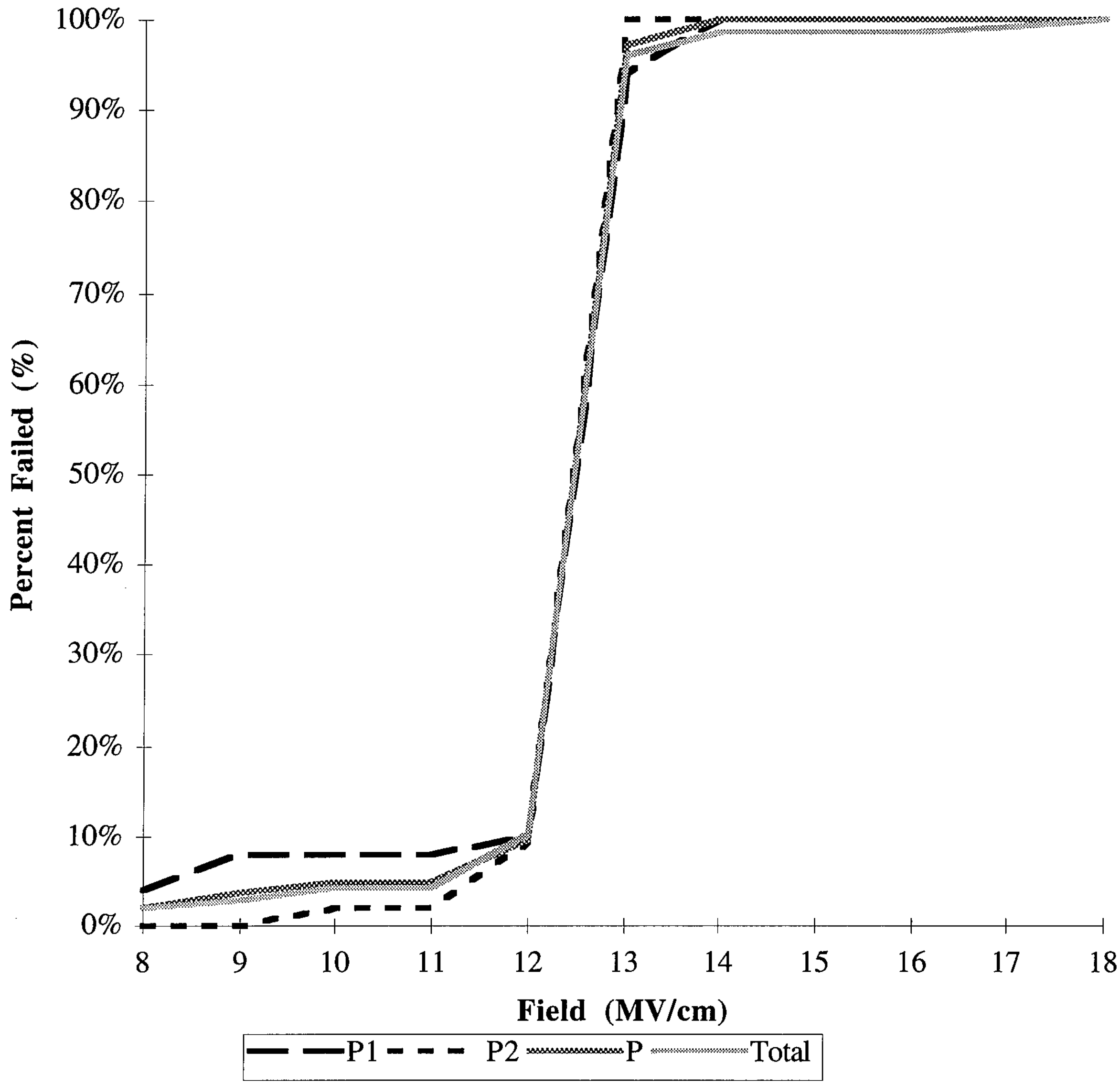

Figure 175. Uncensored Vendor B cumulative breakdown curve for the p capacitors by sample population.

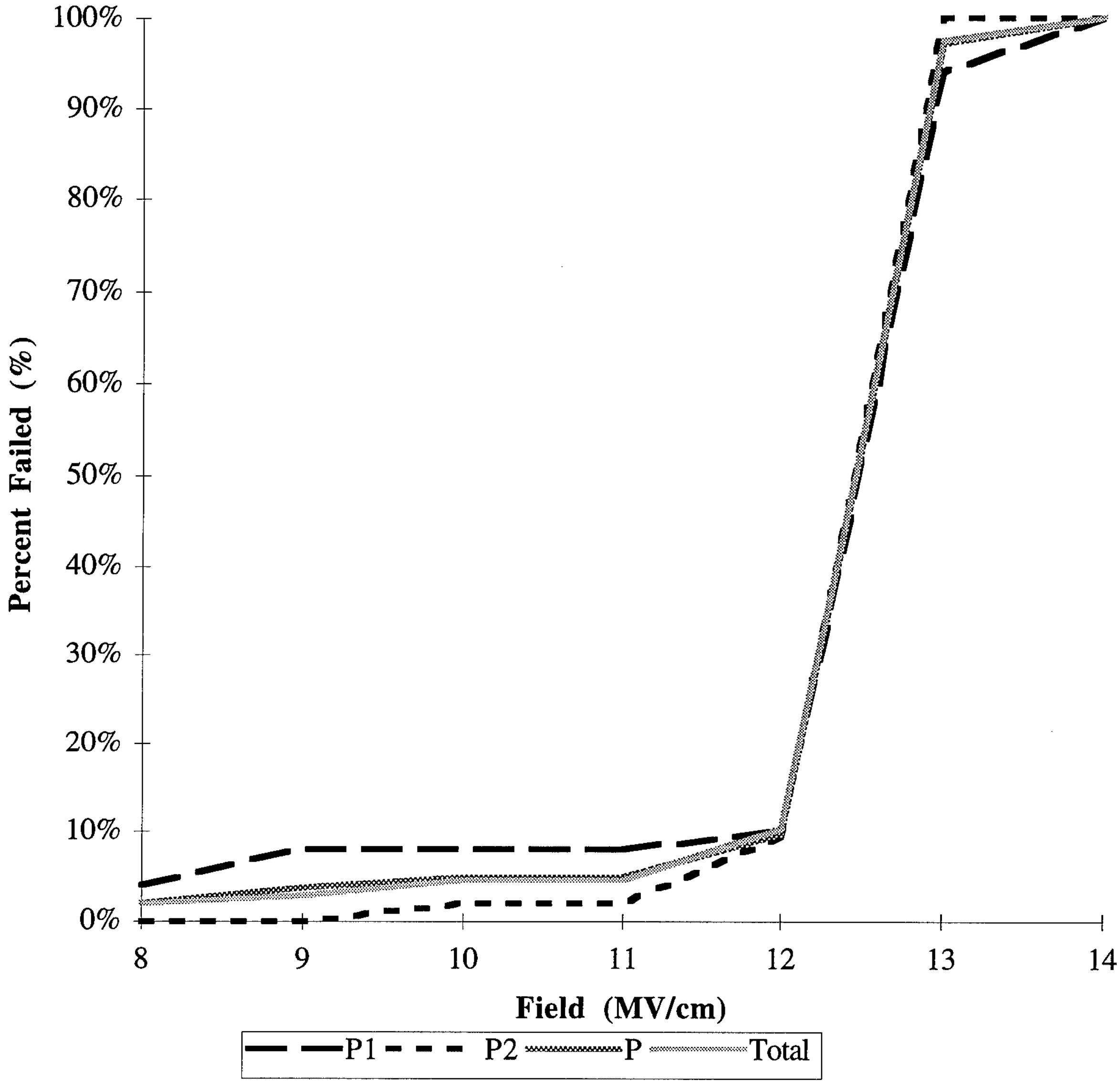

Figure 176. Censored Vendor B cumulative breakdown curve for the p capacitors by sample population.

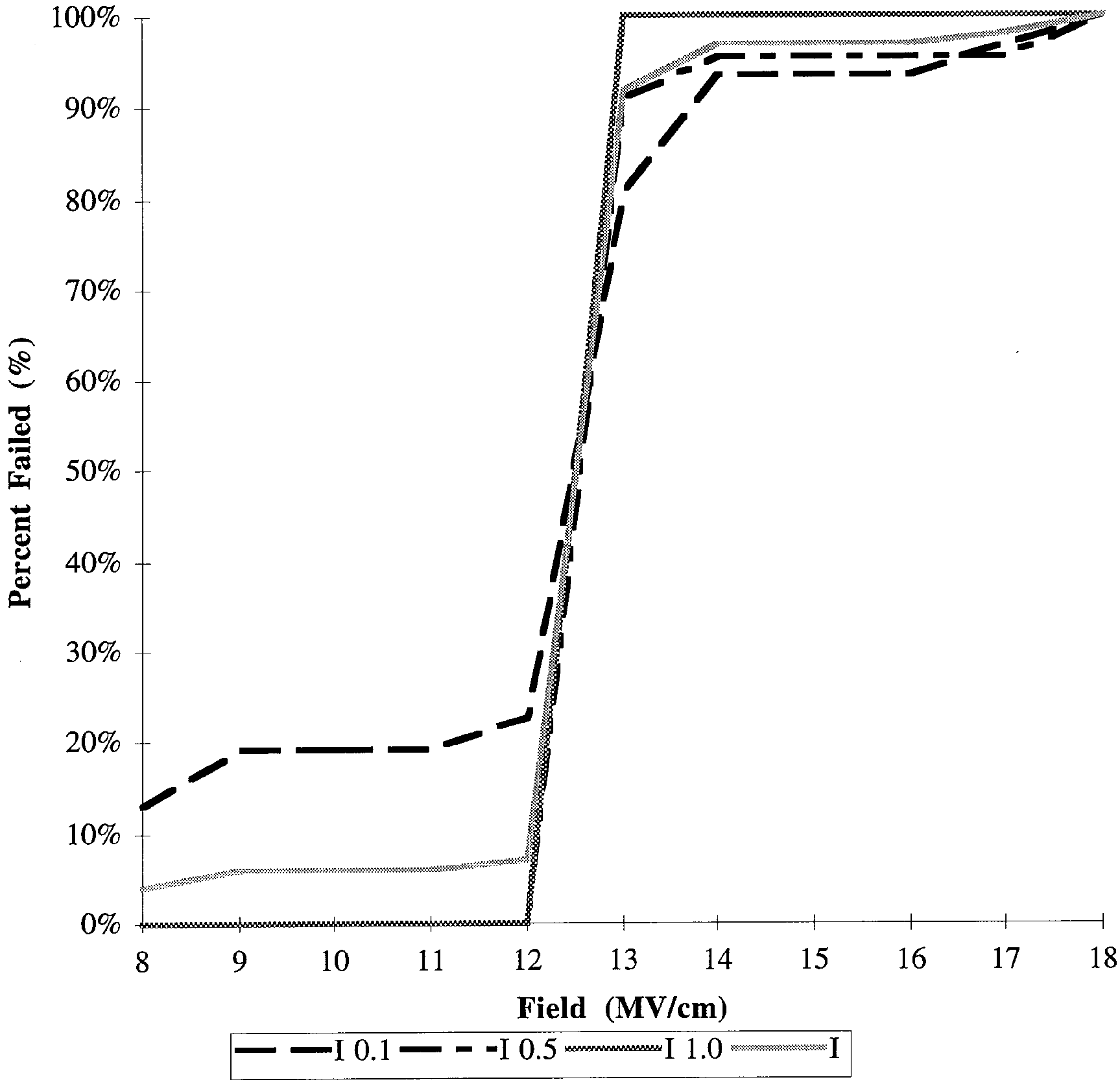

Figure 177. Uncensored Vendor B cumulative breakdown curve for wafer 1 by ramp rate.

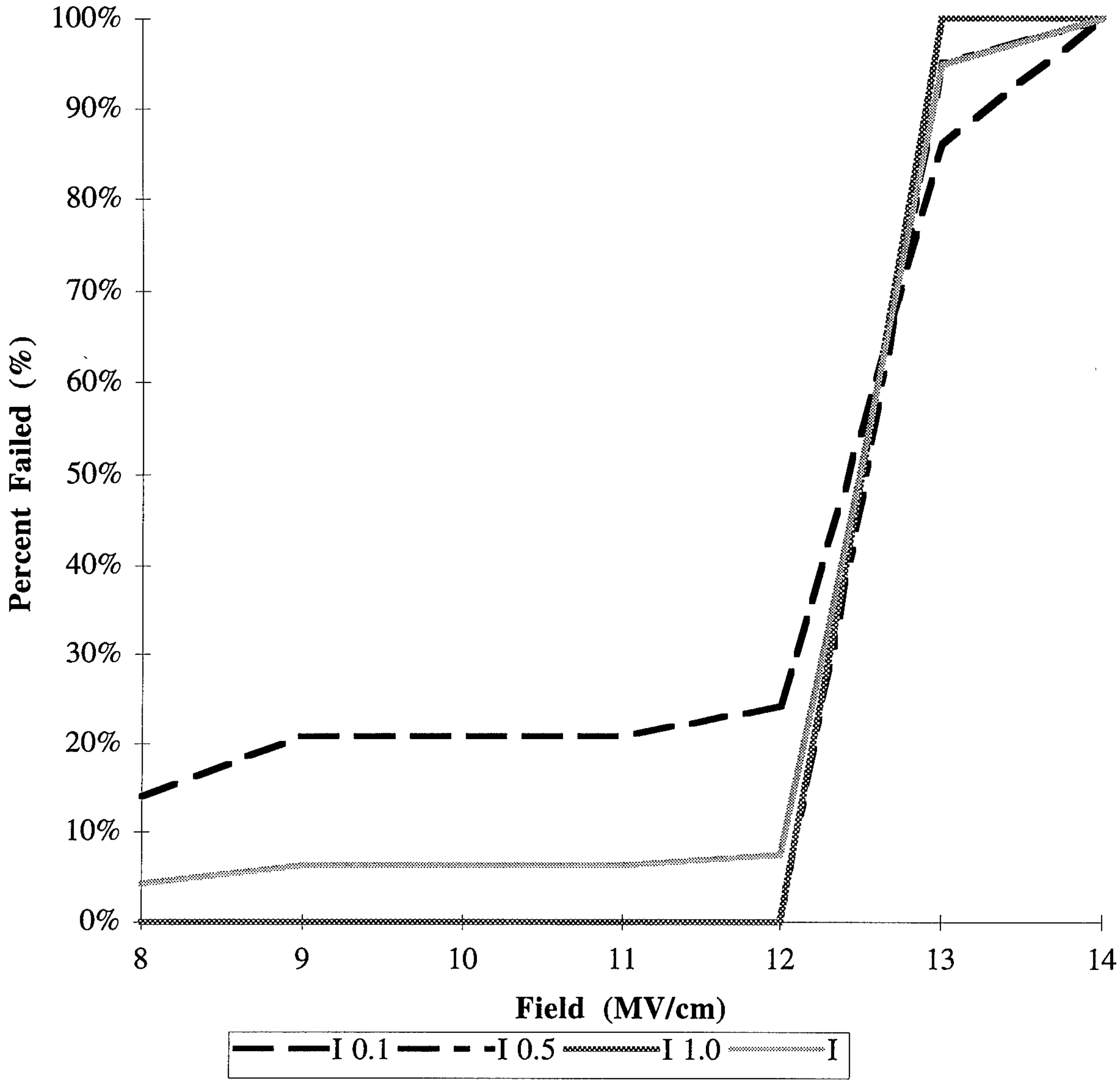

Figure 178. Censored Vendor B cumulative breakdown curve for wafer 1 by ramp rate.

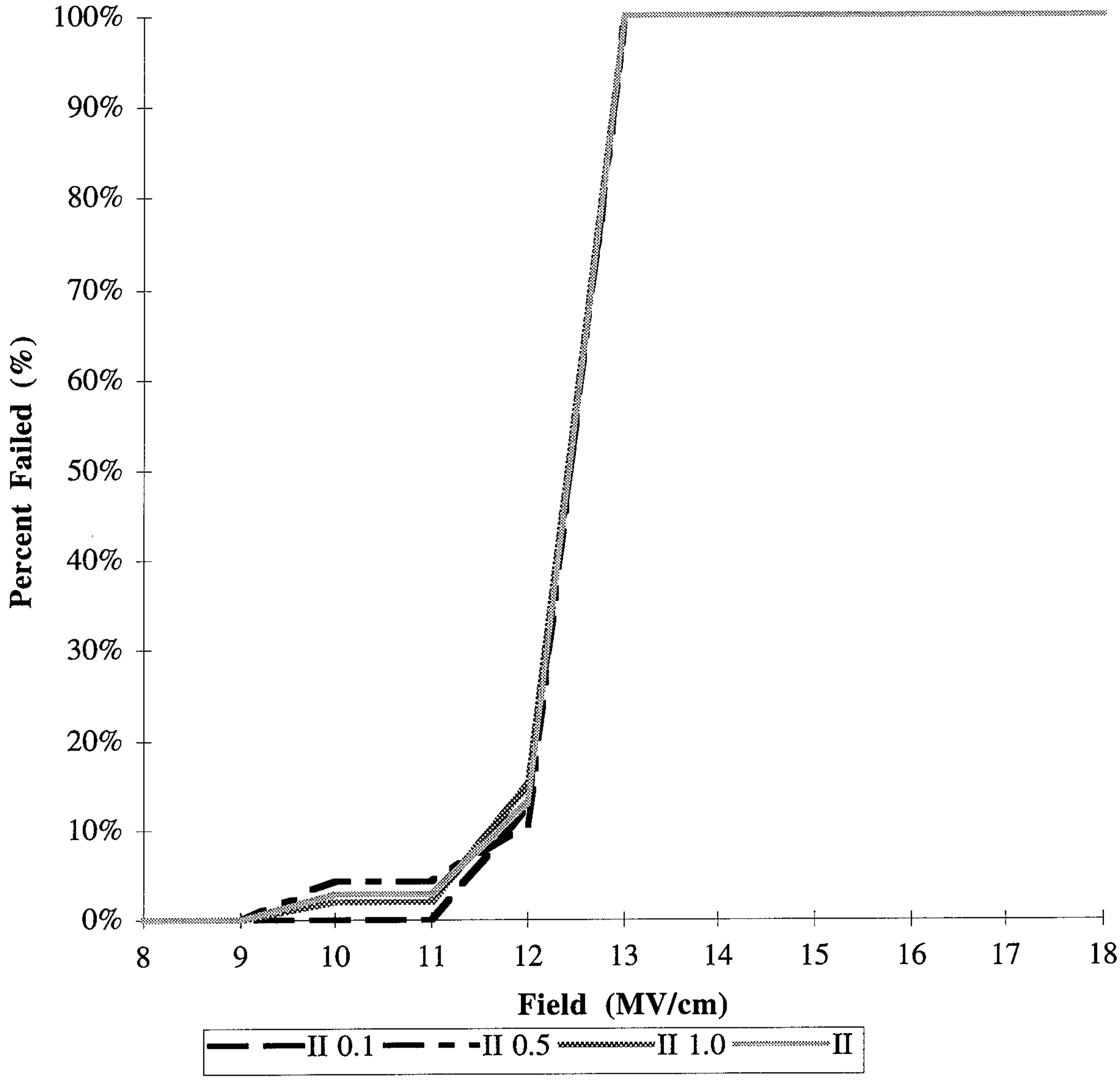

Figure 179. Uncensored Vendor B cumulative breakdown curve for wafer 2 by ramp rate.

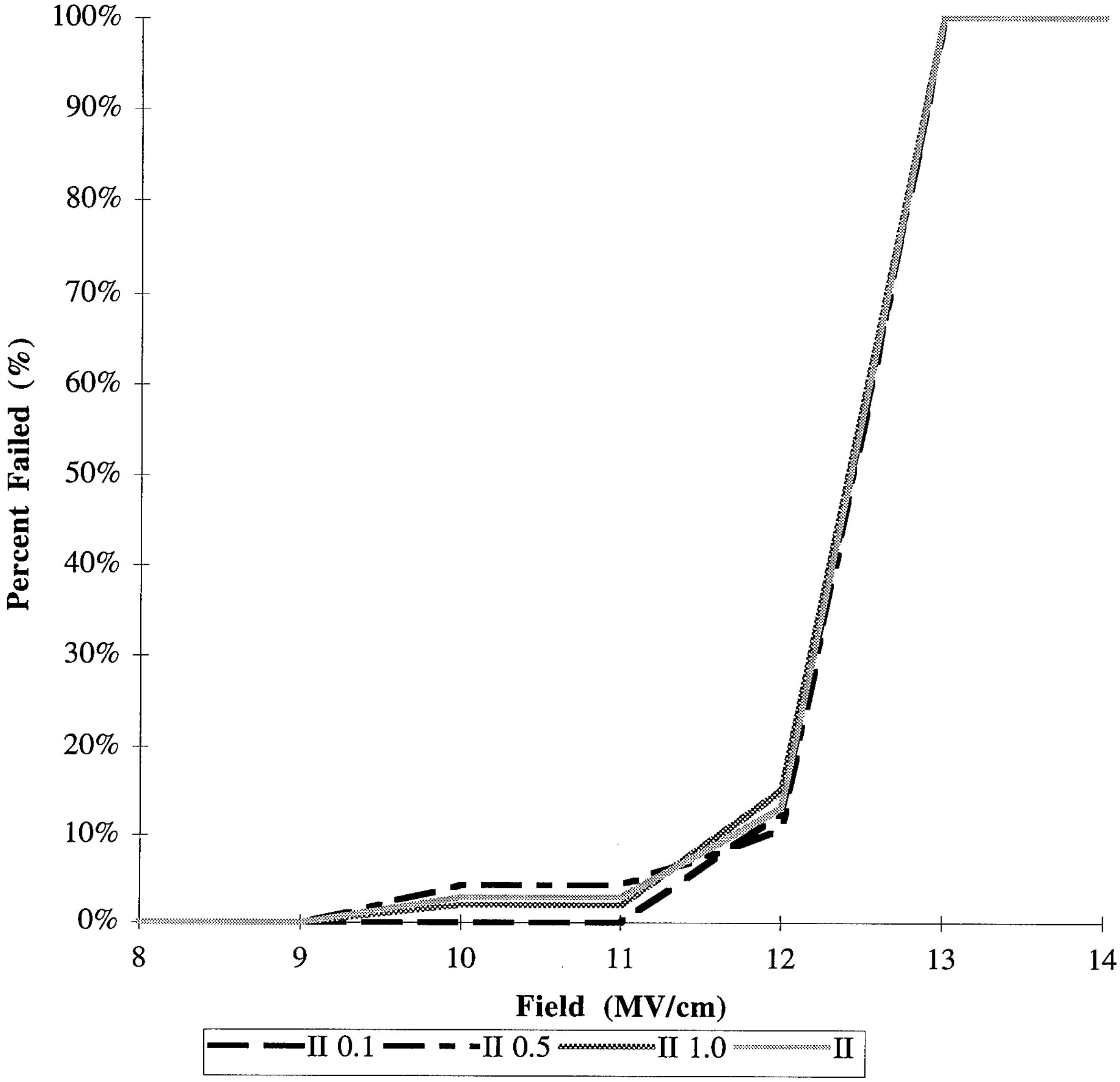

Figure 180. Censored Vendor B cumulative breakdown curve for wafer 2 by ramp rate.

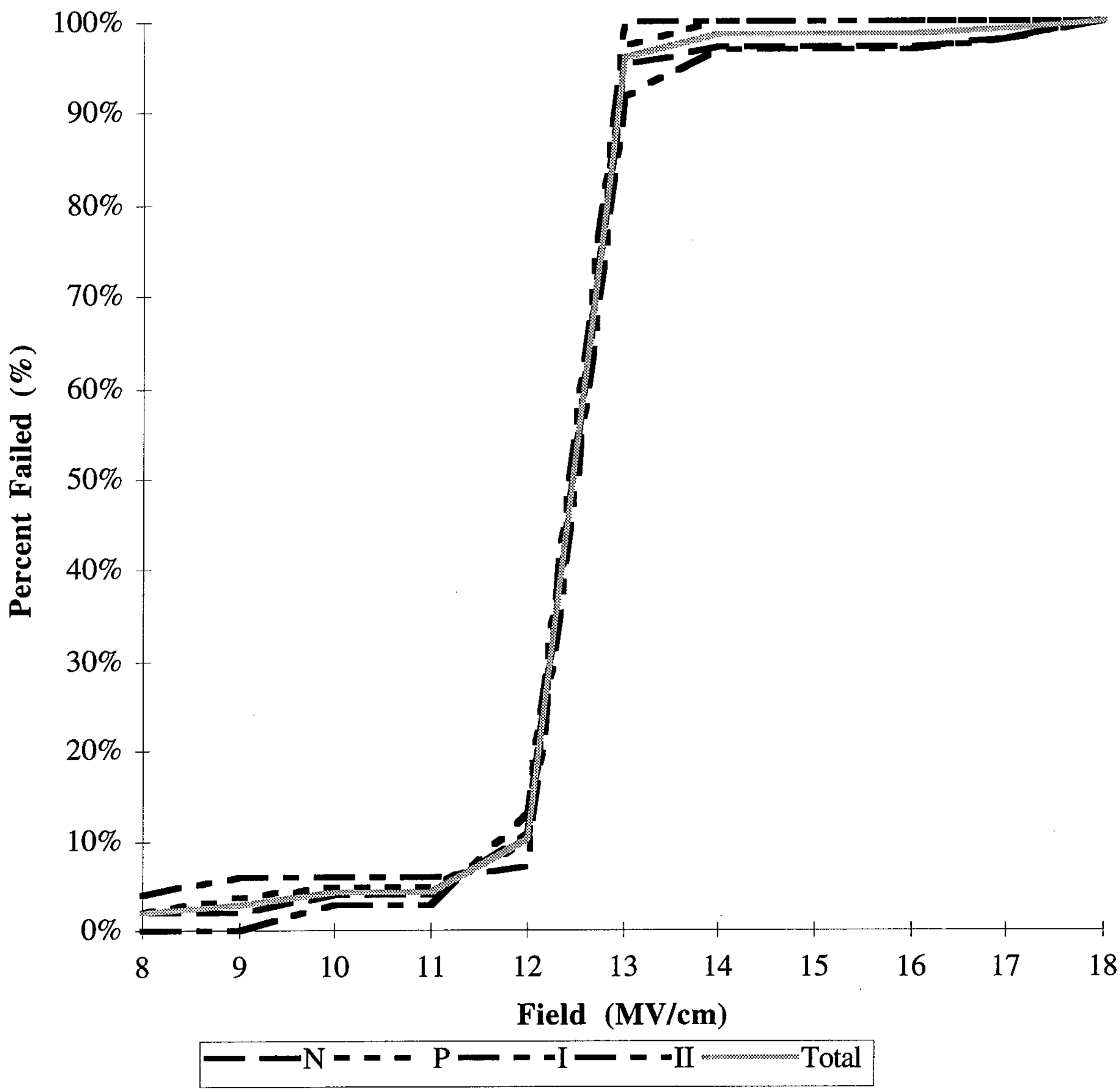

Figure 181. Uncensored Vendor B cumulative breakdown curve by capacitor type and wafer location.

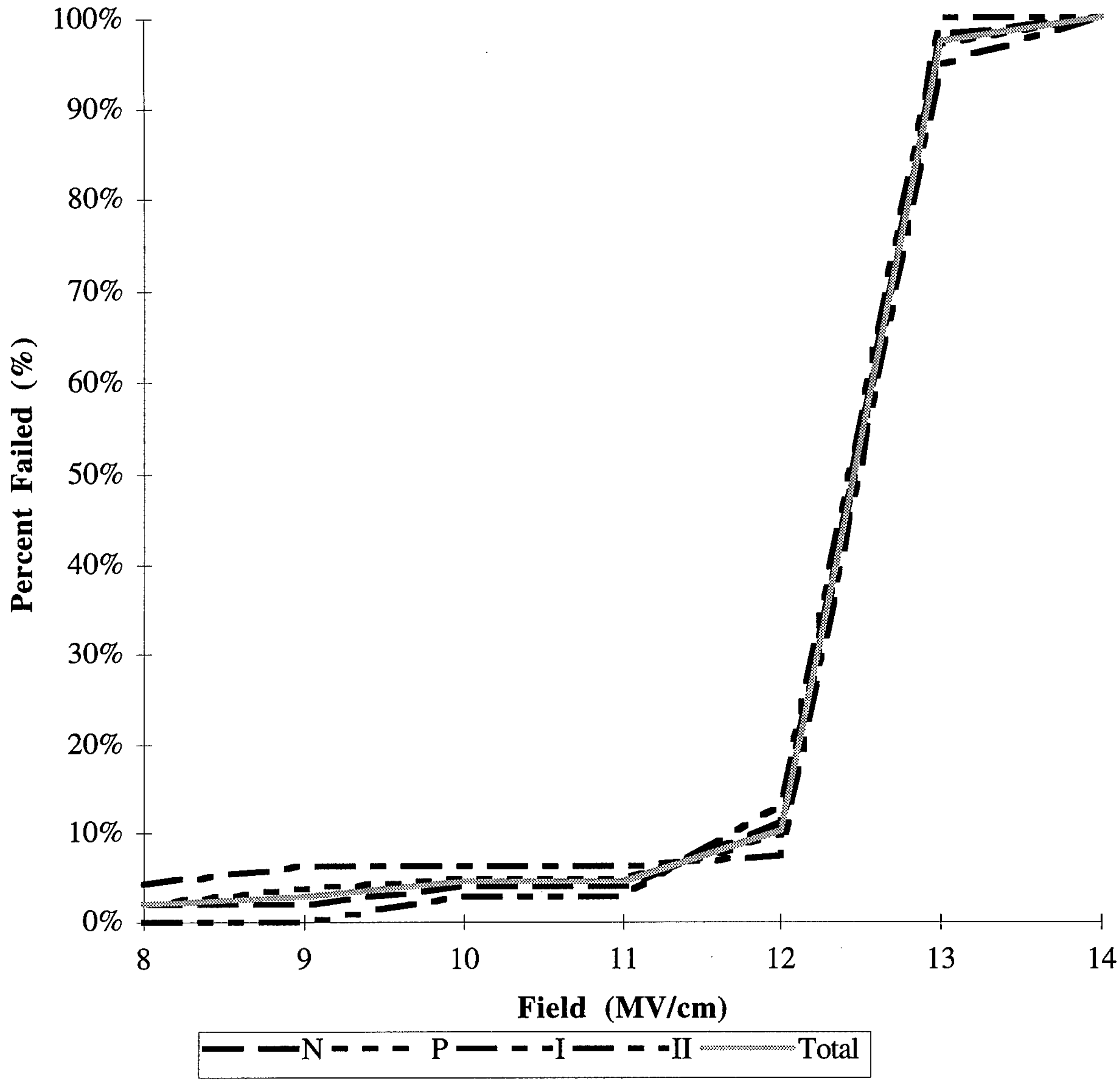

Figure 182. Censored Vendor B cumulative breakdown curve by capacitor type and wafer location.

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